

Figure 1. The Trisect-Decomposing an 18x18 Product Partial Matrix.

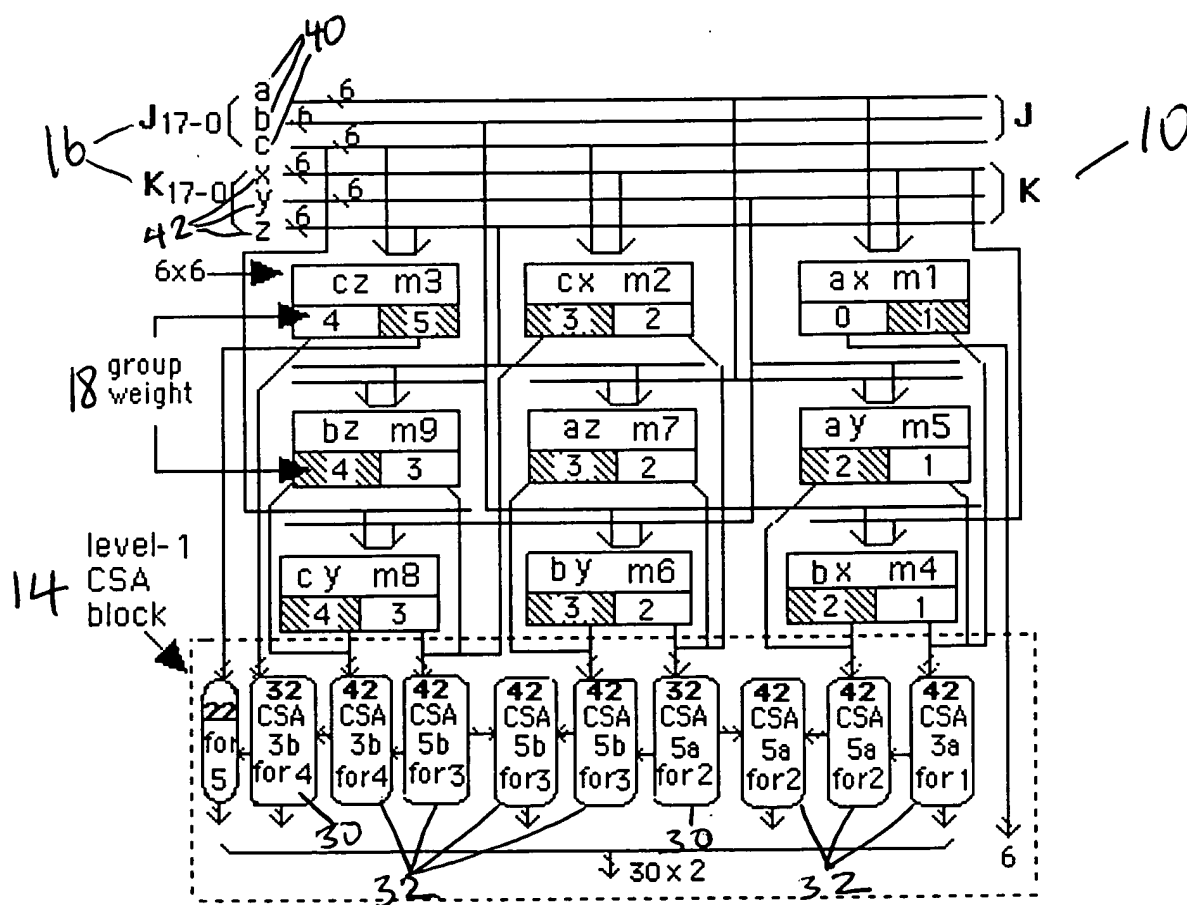
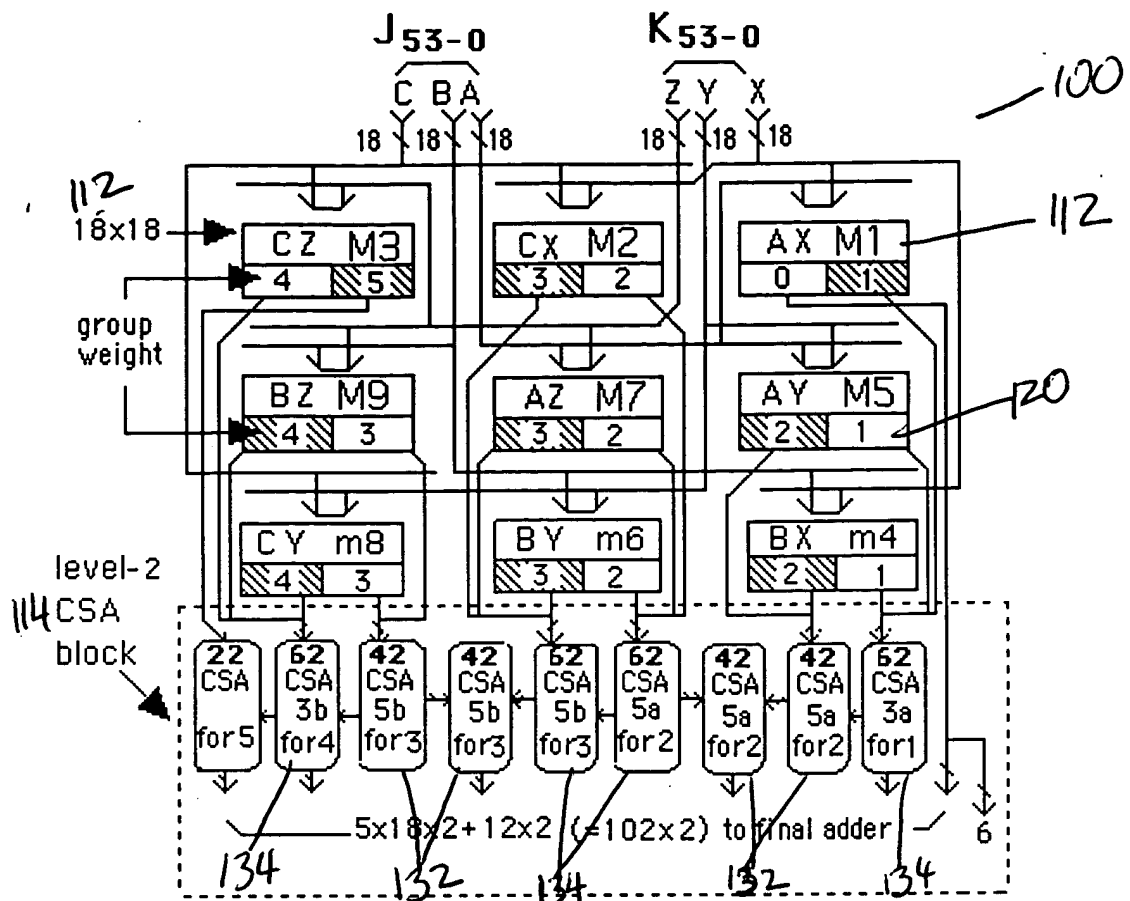


Figure 2. The Triple-Expanded 18x18-b Multiplier  
(The Re-Arrangement of Figure 1 with CSA Outputs).



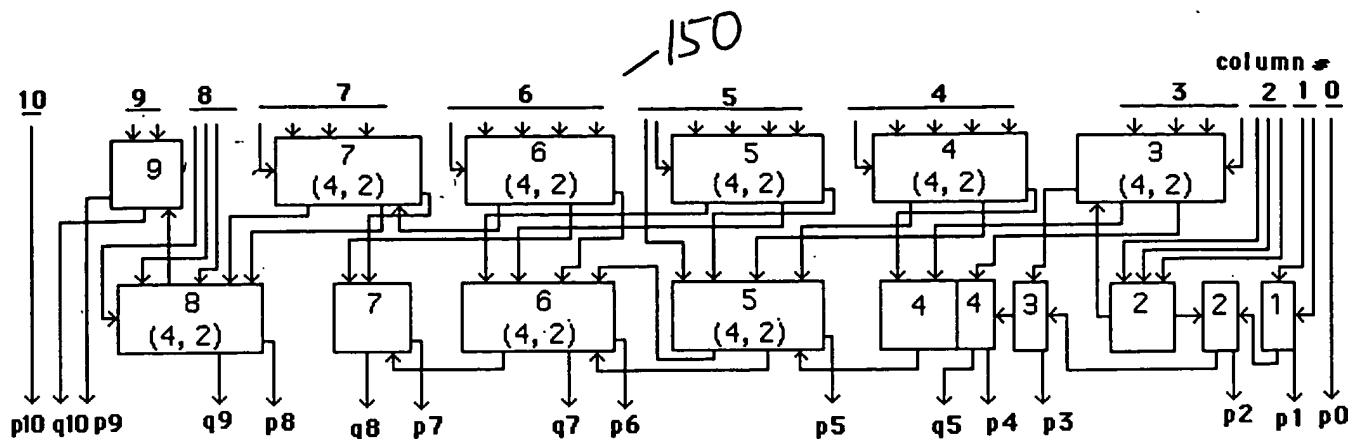


Figure 4a. The 6 x 6-b (4,2)-(3,2) based virtual multiplier (with a rectangular shape).

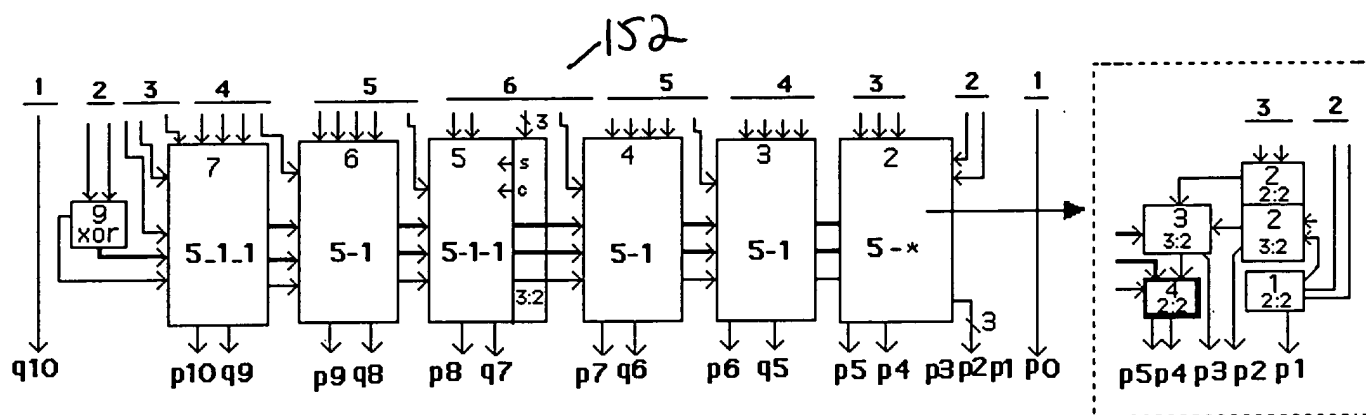


Figure 4b. The 6 x 6-b borrow parallel virtual multiplier.

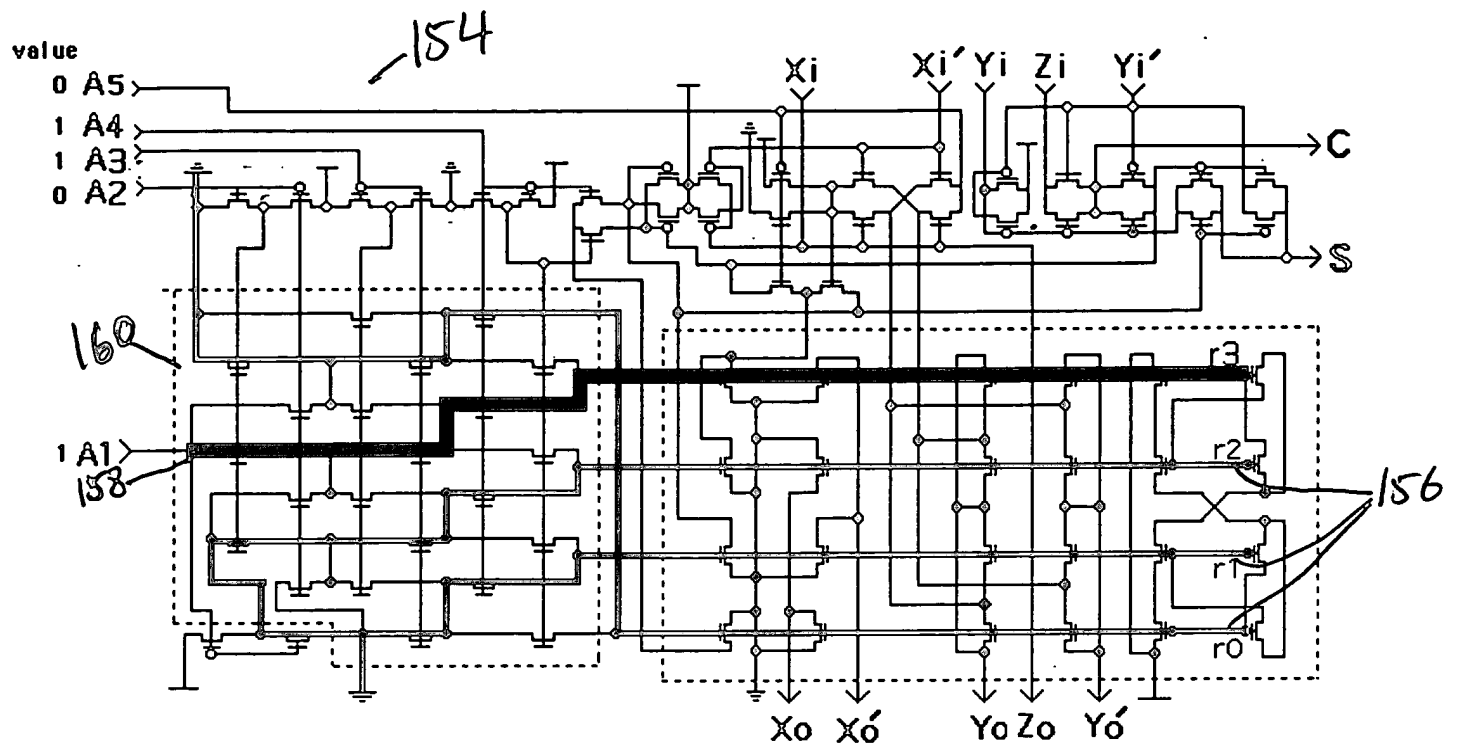


Figure 5 The 5\_1 borrow parallel counter.  $R=(r_0 \ r_1 \ r_2 \ r_3)$  is a 4-b 1-hot encoded signal.  $A_5$  is a borrow bit,  $X_i/X_o$ ,  $Y_i/Y_o$ ,  $Z_i/Z_o$  are in-stage in/out bits.

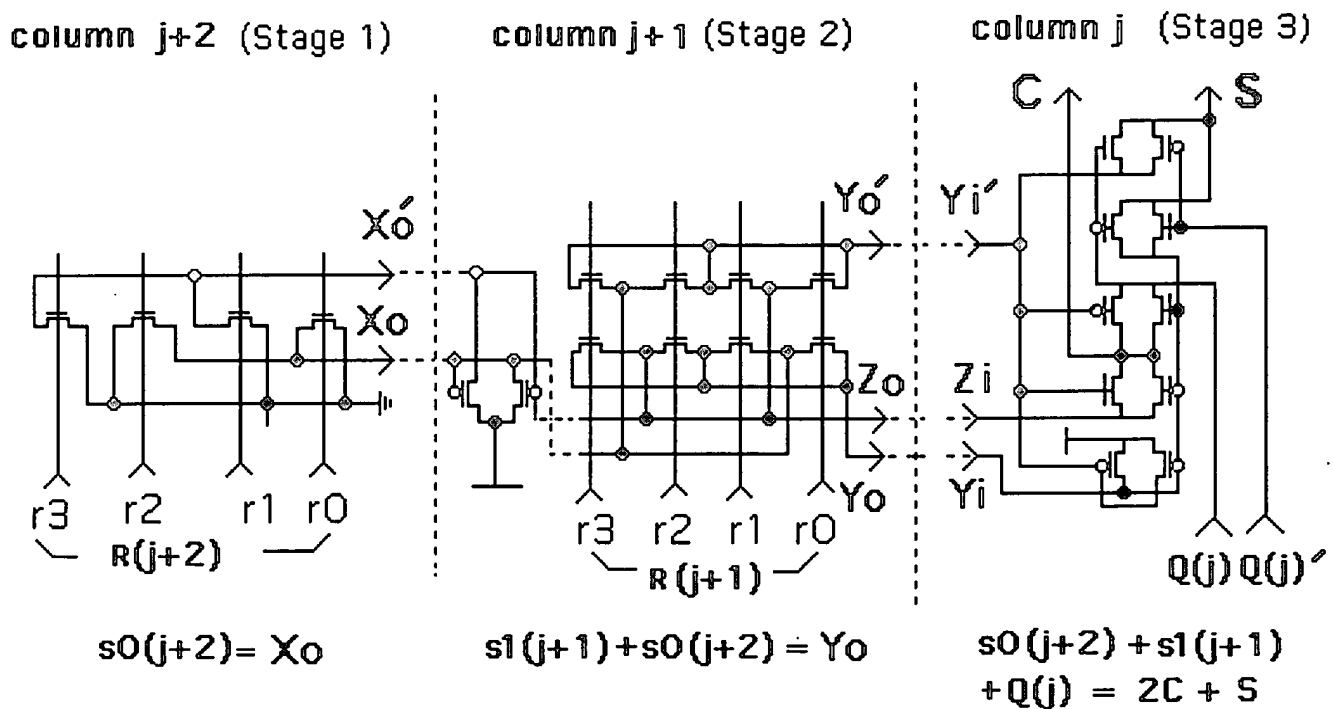


Figure 6 The full adder adding three bits, one binary and two 4-b 1-hot encoded bits, without type conversion.

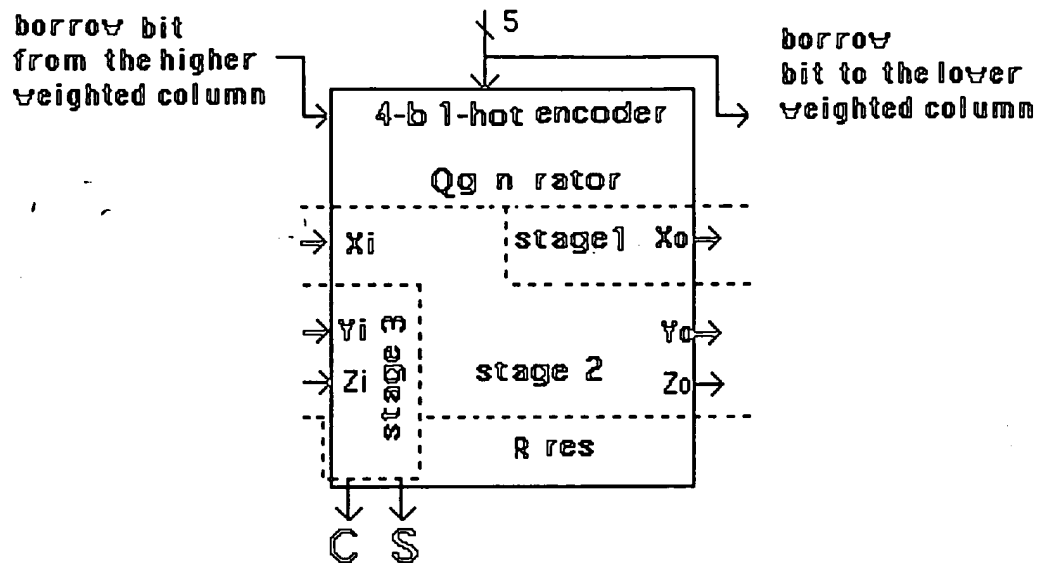


Figure 7. The functional structure of the 5\_1 parallel counter.

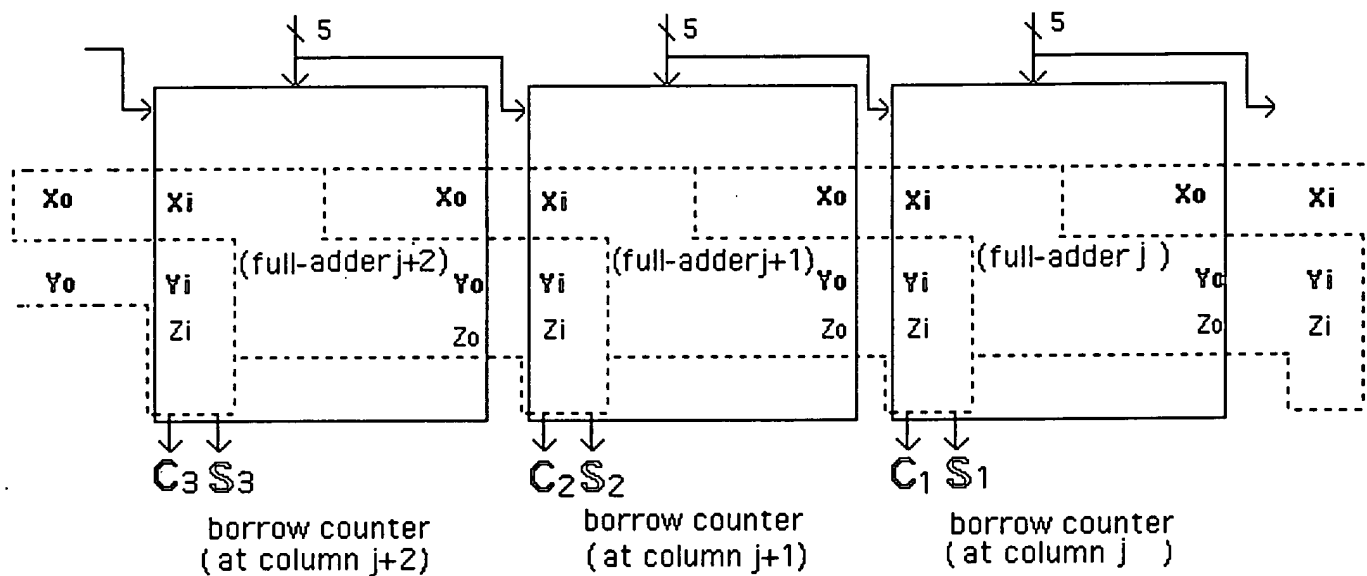


Figure 8. A typical application of 5\_1 counter array.

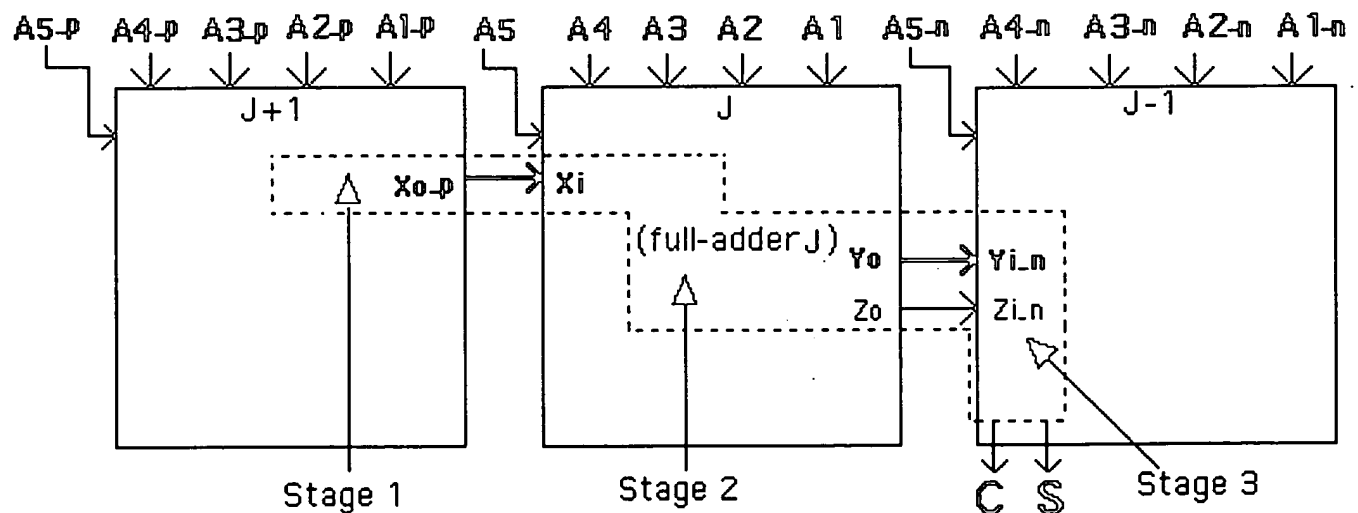


Figure 9. A full-adder embedded in three contiguous borrow parallel counters.

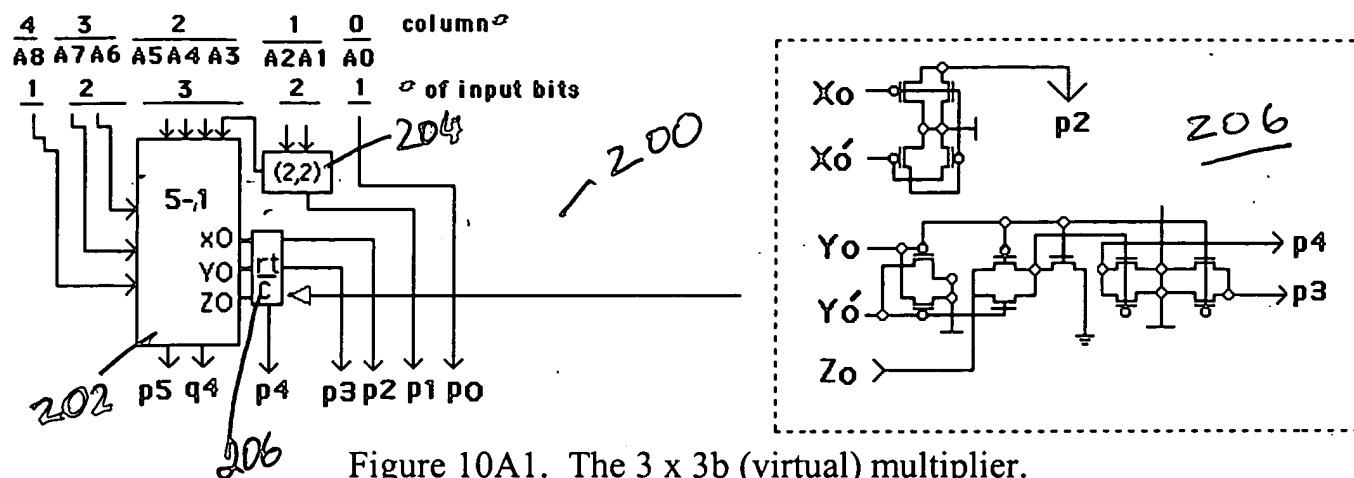


Figure 10A1. The 3 x 3b (virtual) multiplier.

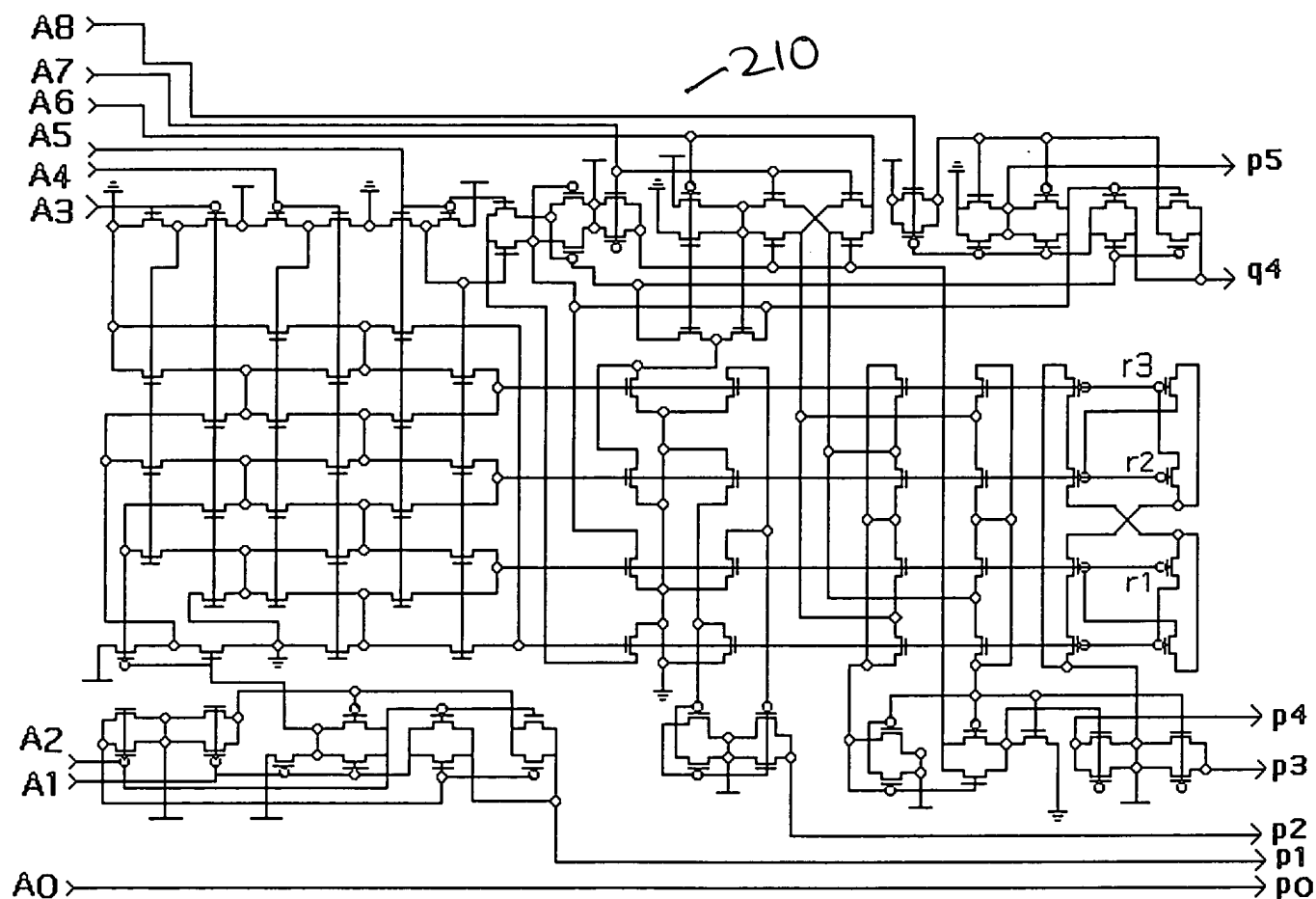


Figure 10A2. The 3x3 (virtual) multiplier circuit.

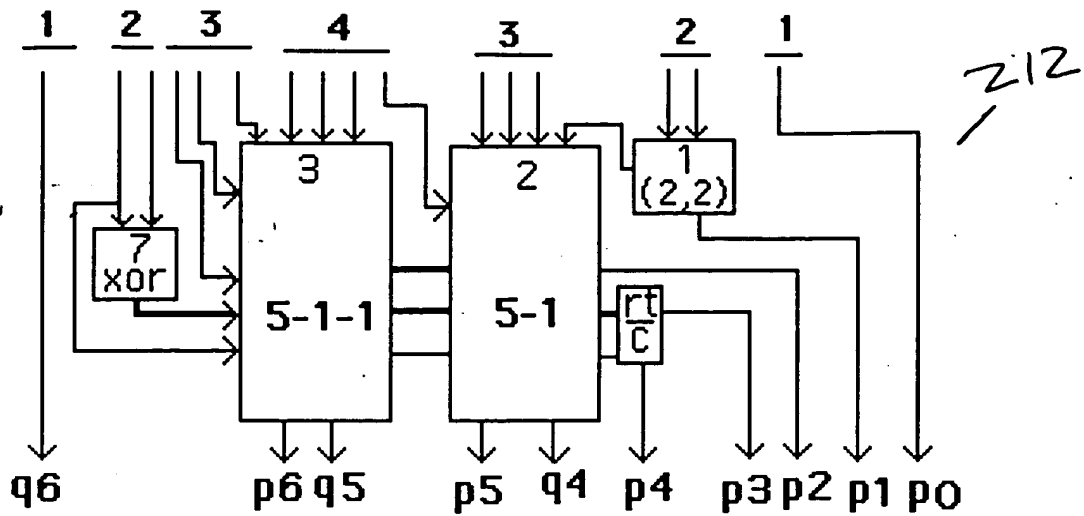


Figure 10A3. The 4x4 virtual multiplier.

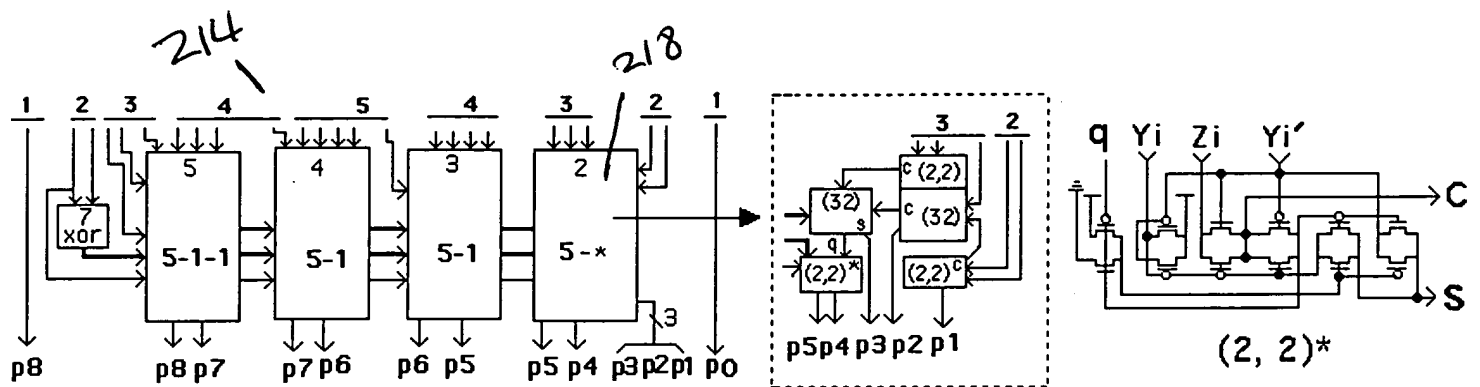


Figure 10A4. The 5x5a (virtual) multiplier.

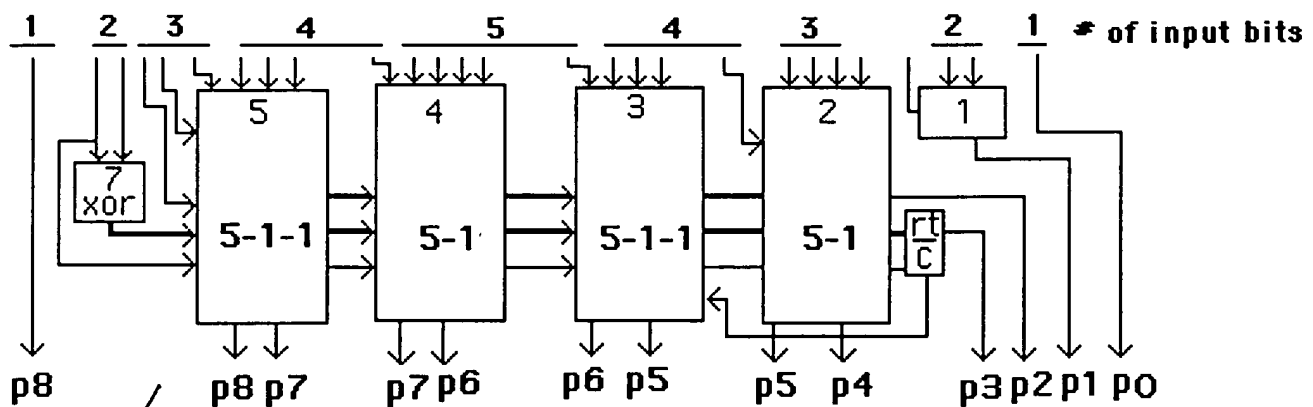


Figure 10A5. The 5x5b (virtual) multiplier.

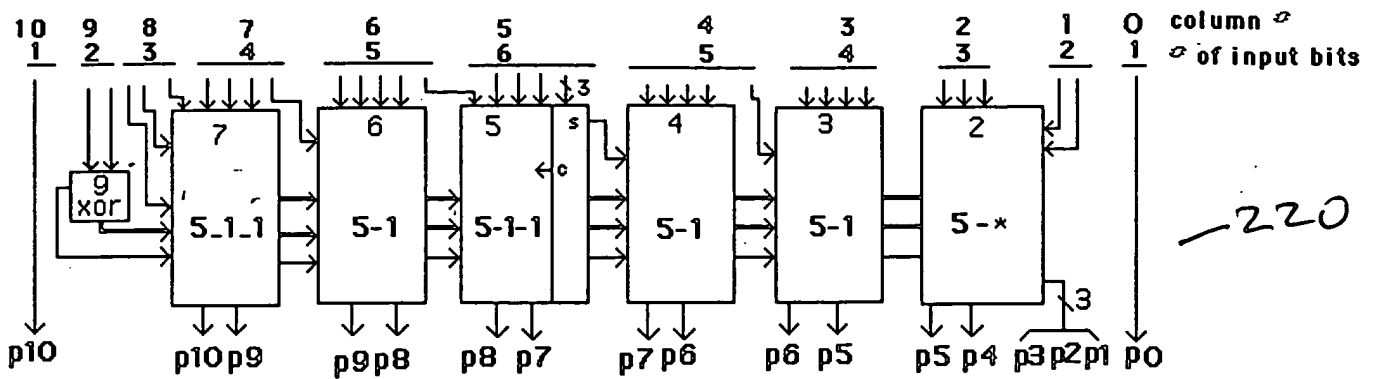


Figure 10A6. The 6x6a (virtual) multiplier.

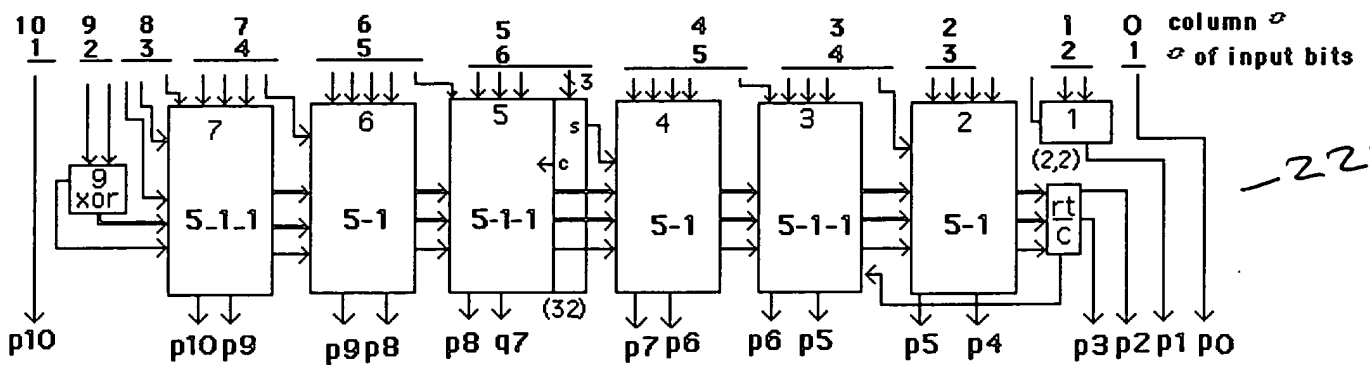


Figure 10A7. The 6x6b (virtual) multiplier.

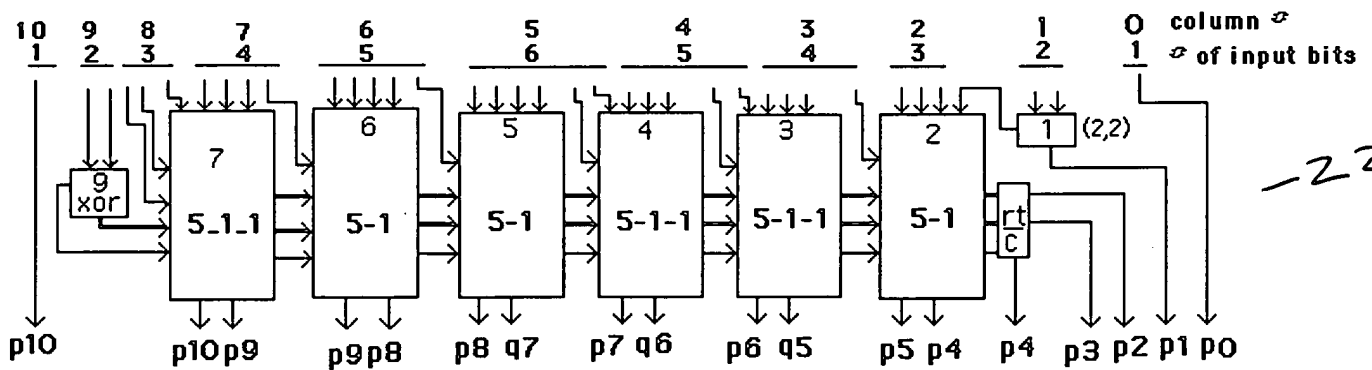


Figure 10A8. The 6x6c (virtual) multiplier.



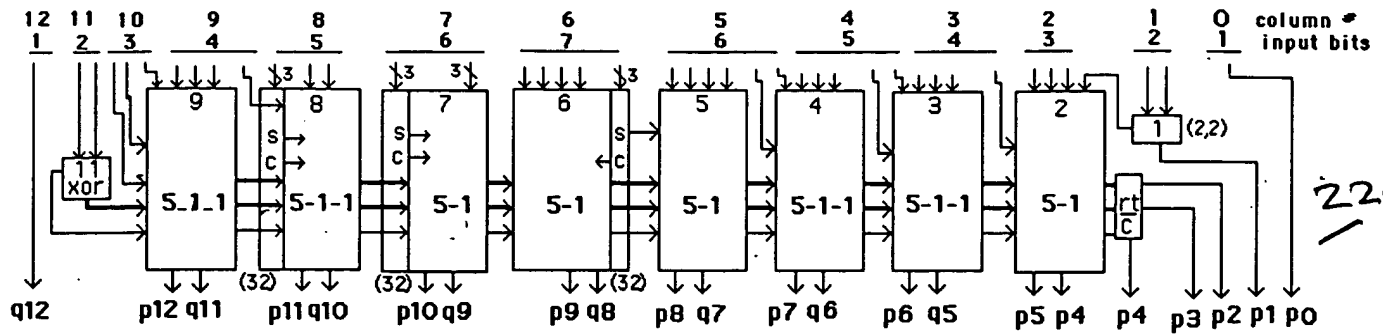


Figure 10A9. The 7x7 (virtual) multiplier.

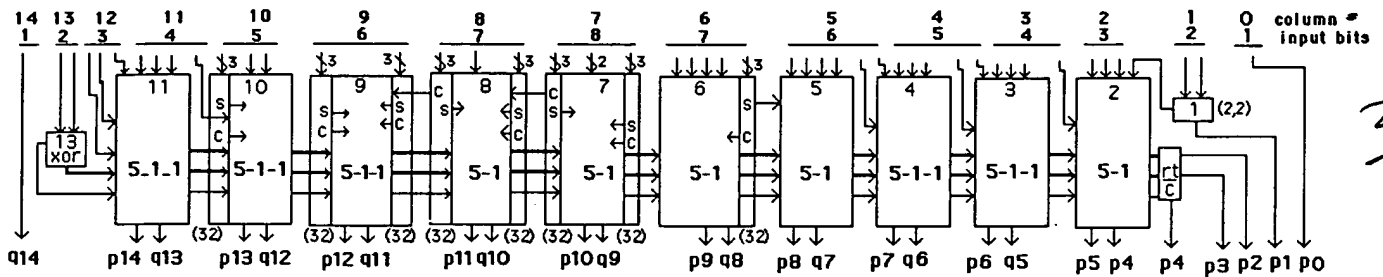


Figure 10A10. The 8x8 (virtual) multiplier.

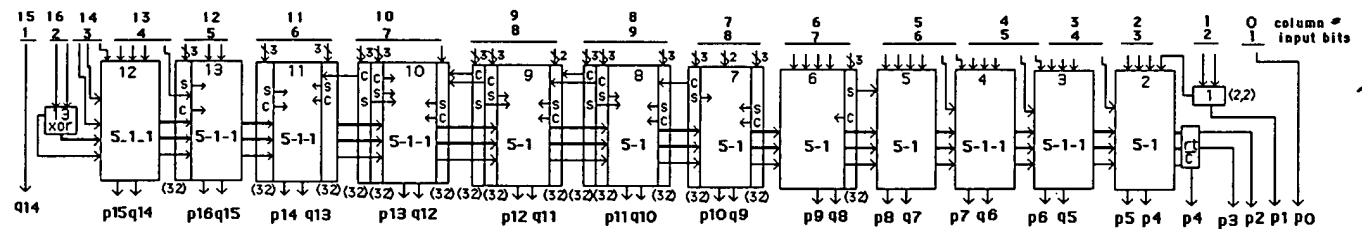


Figure 10A11. The 9x9 (virtual) multiplier.

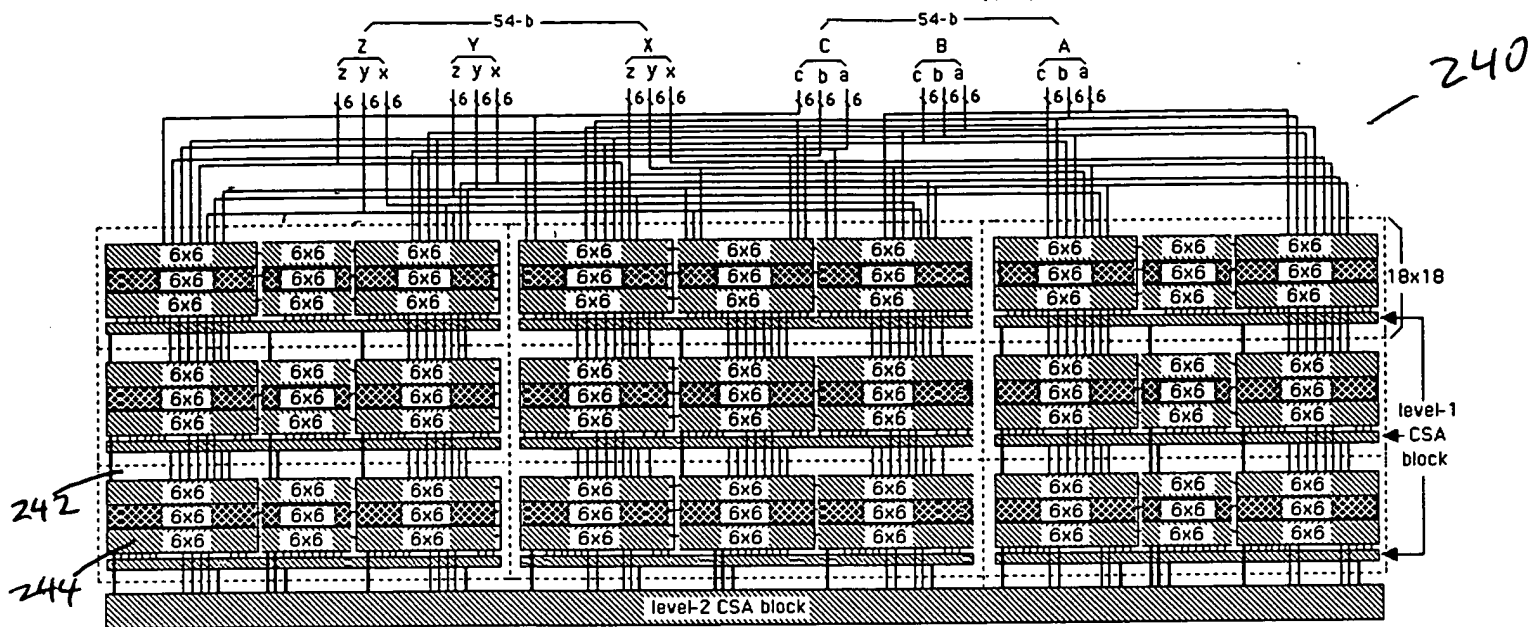
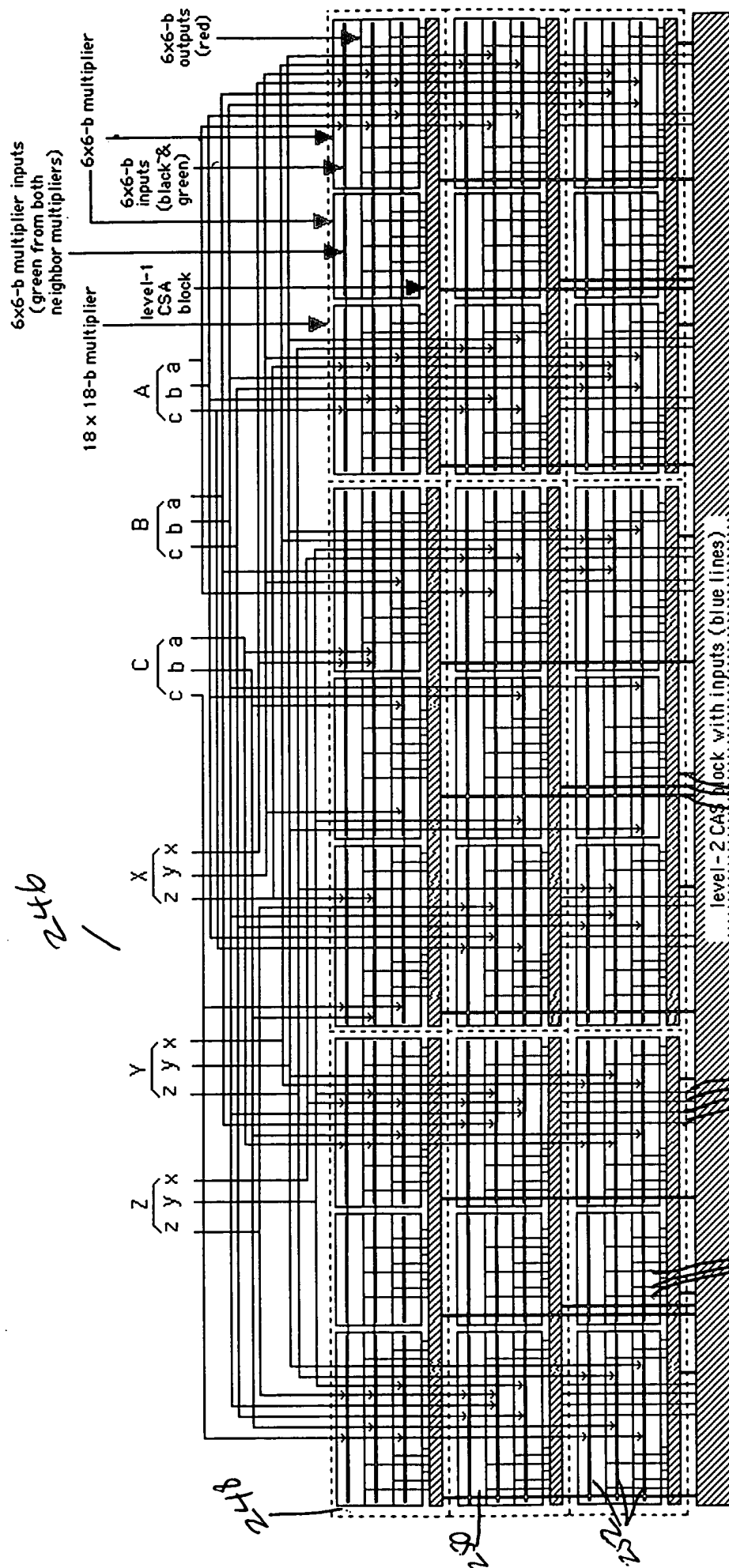
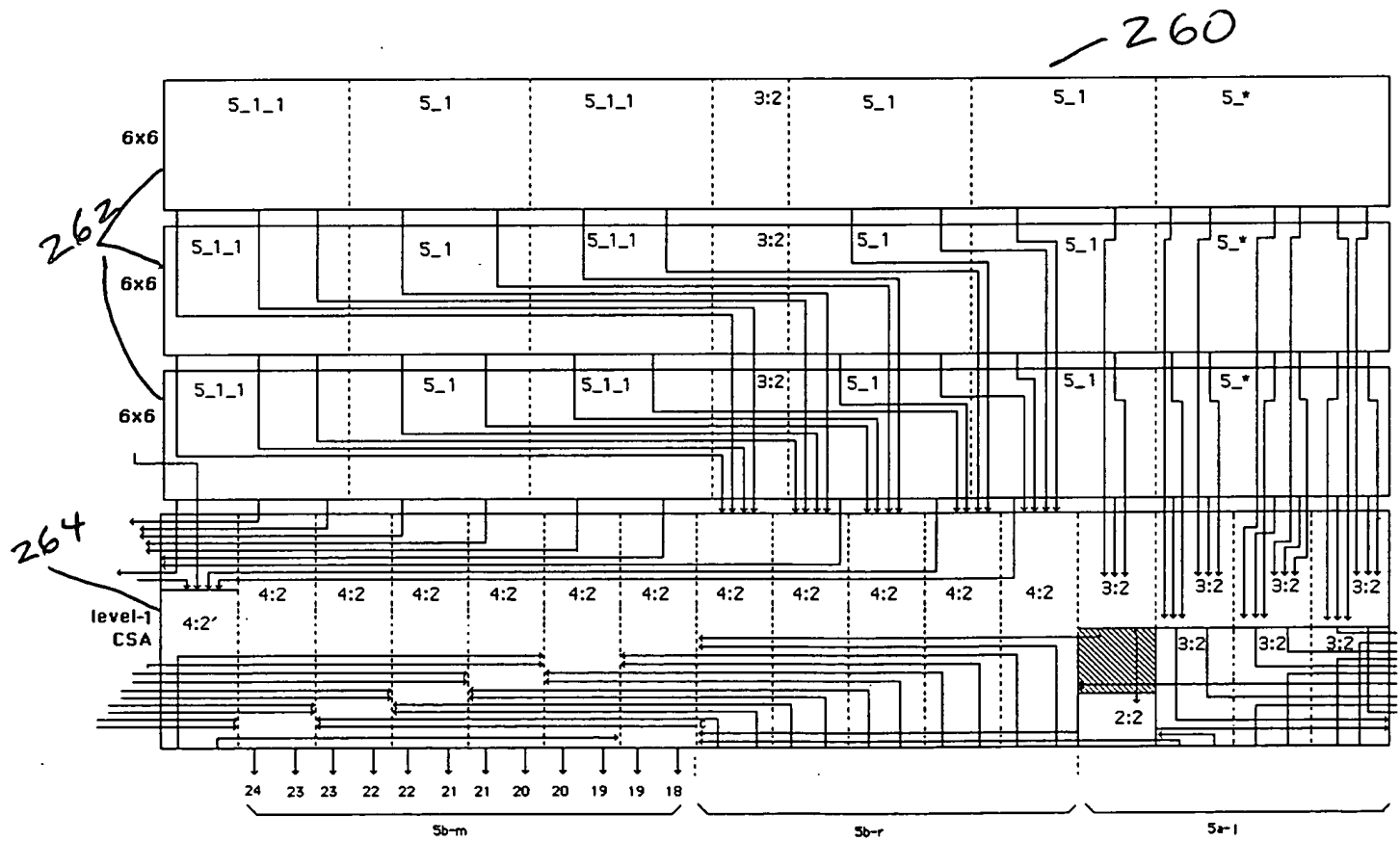
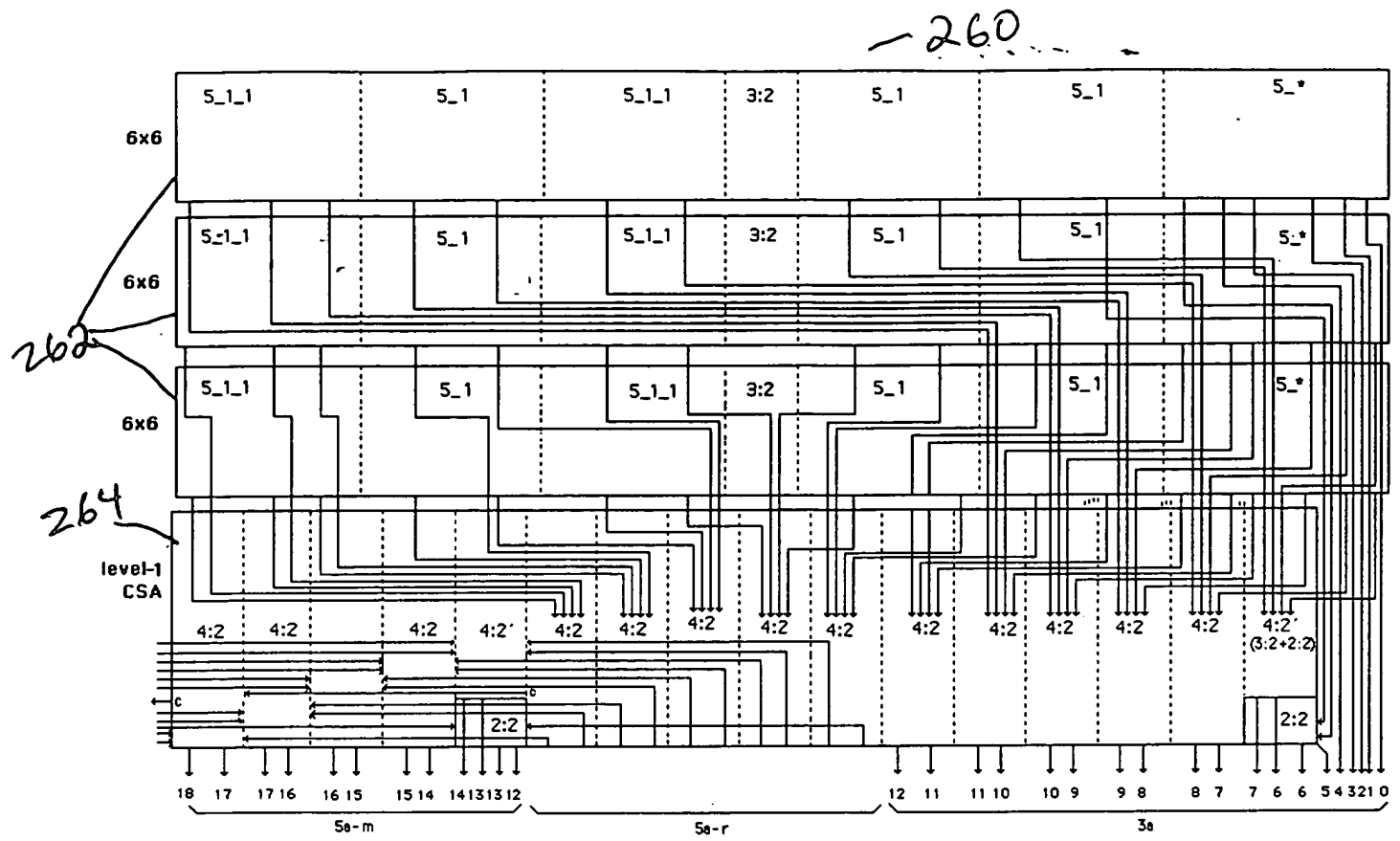


Figure 10B1. The organization 54x 54 triple-expanded multiplier with 2-levels of CSAs



**Figure B2.** (colored drawing) The internal connects of the 54 x 54-b triple-expanded multiplier. All 18x18-b (as well as 6x6-b) sub-multipliers are identical, except the input/output and connection lines. Input lines (in black) and lines from each base multiplier to level-1 CSA blocks (in red) are all 6-b each. Lines from level-1 to level-2 CSA blocks (in blue) are 6-bit for each single line and 24-b for each block line.



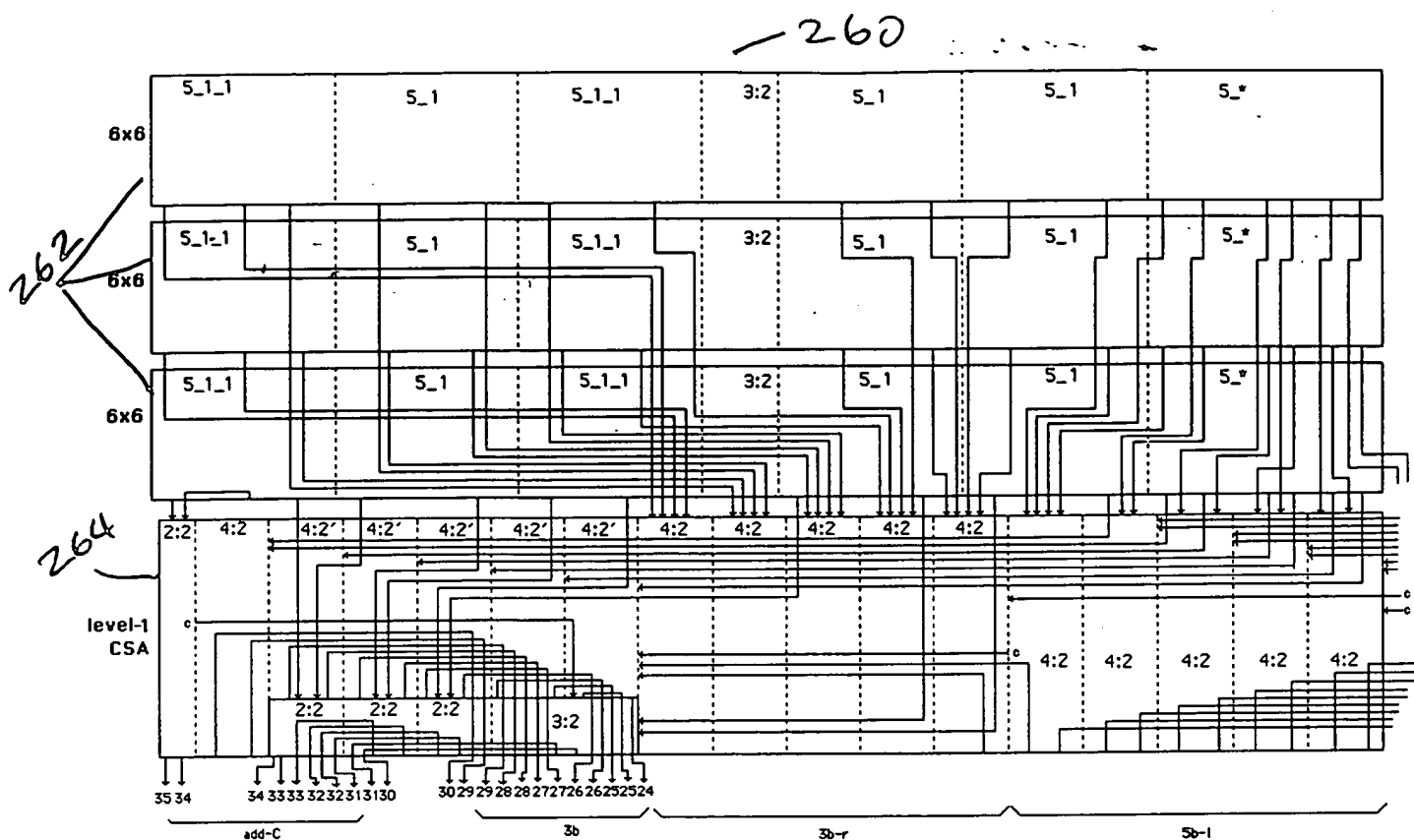


Figure 10B5. Left-side of the 18x18 Multiplier.

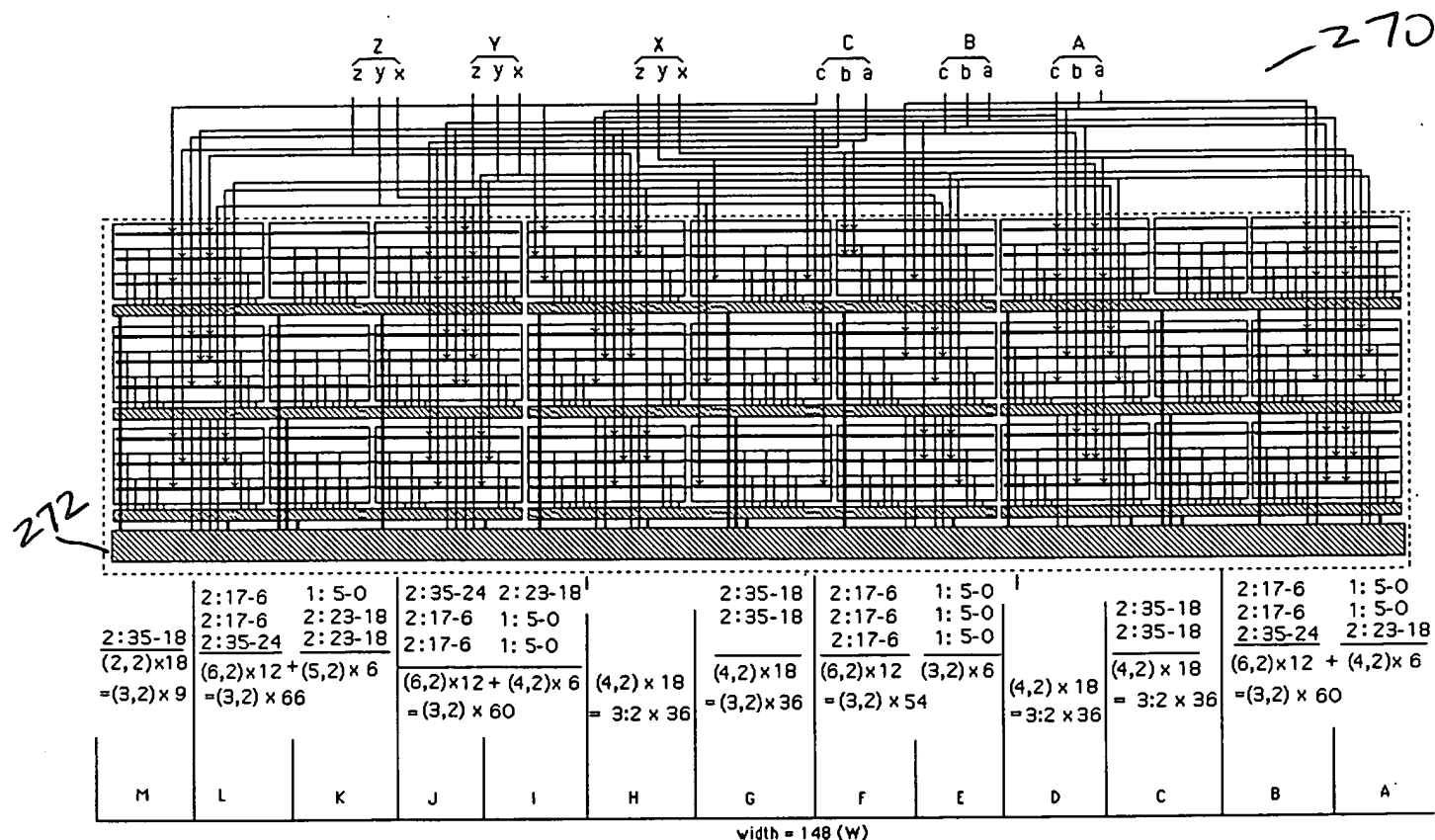


Figure 10B6. Level-2 CSA of the 54 x 54 Multiplier.

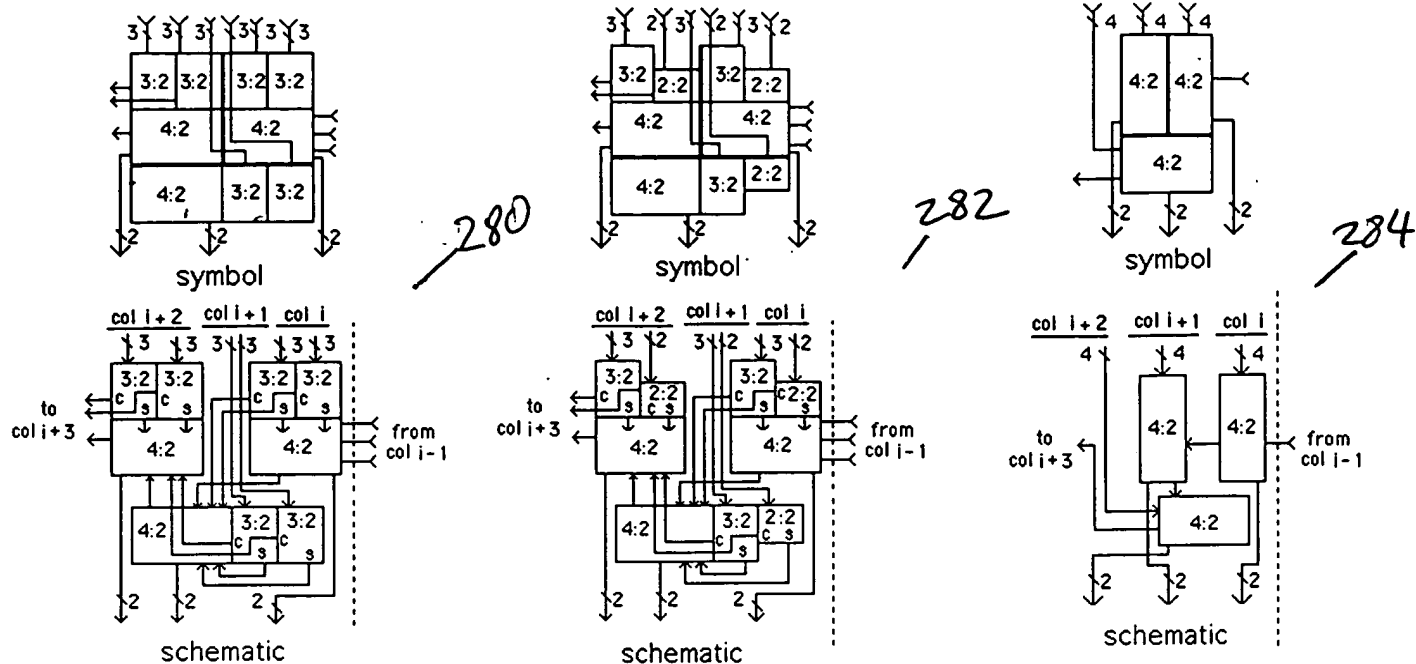


Figure 10B7. The definitions of binary counter blocks.

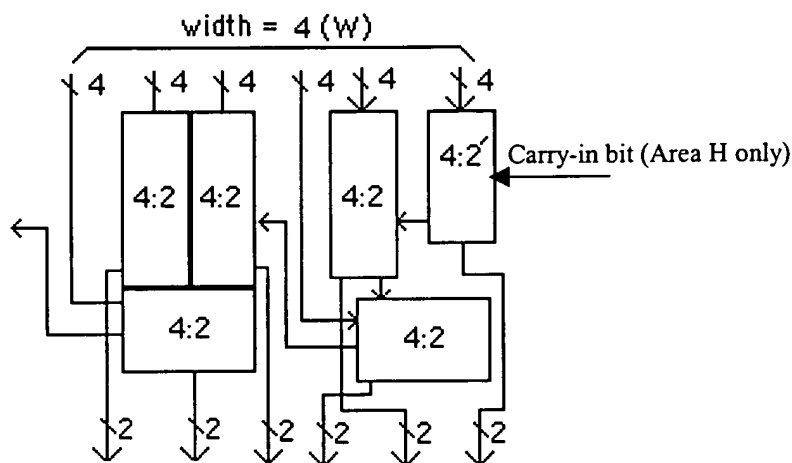


Figure 10B8. The layout draft for areas A, D, and H.

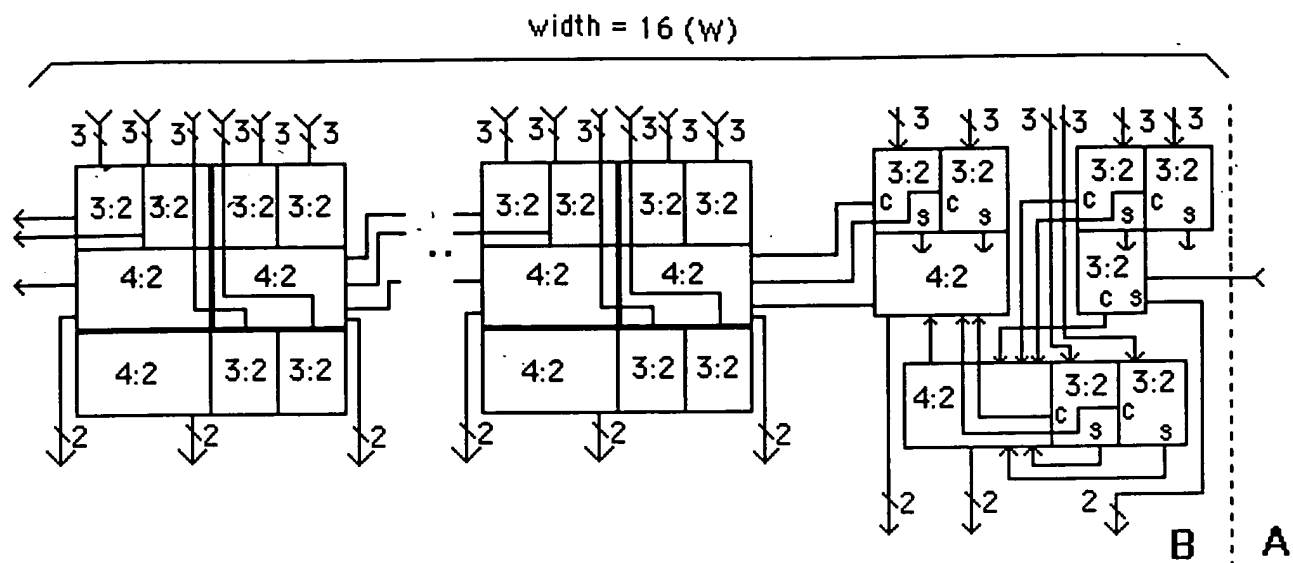


Figure 10B9. The layout draft for area B and F.

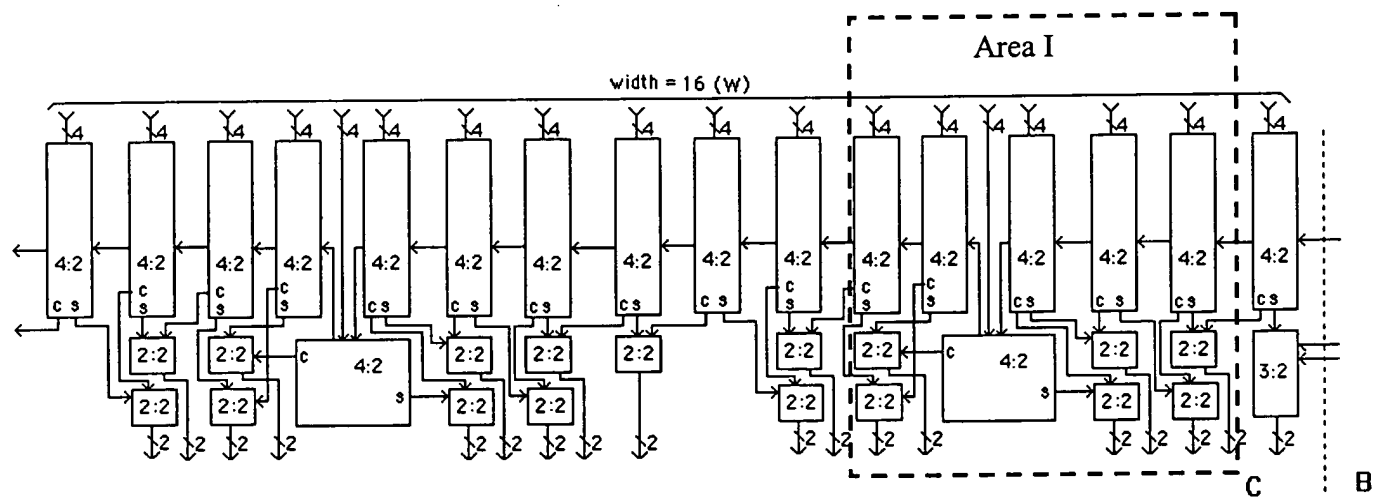


Figure 10B10. The layout draft for areas C, G, and I.

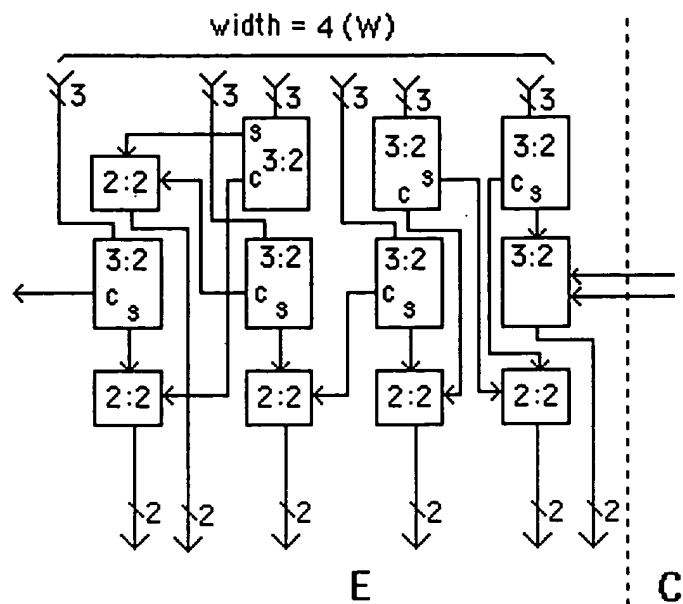


Figure 10B11. The layout draft for area E.

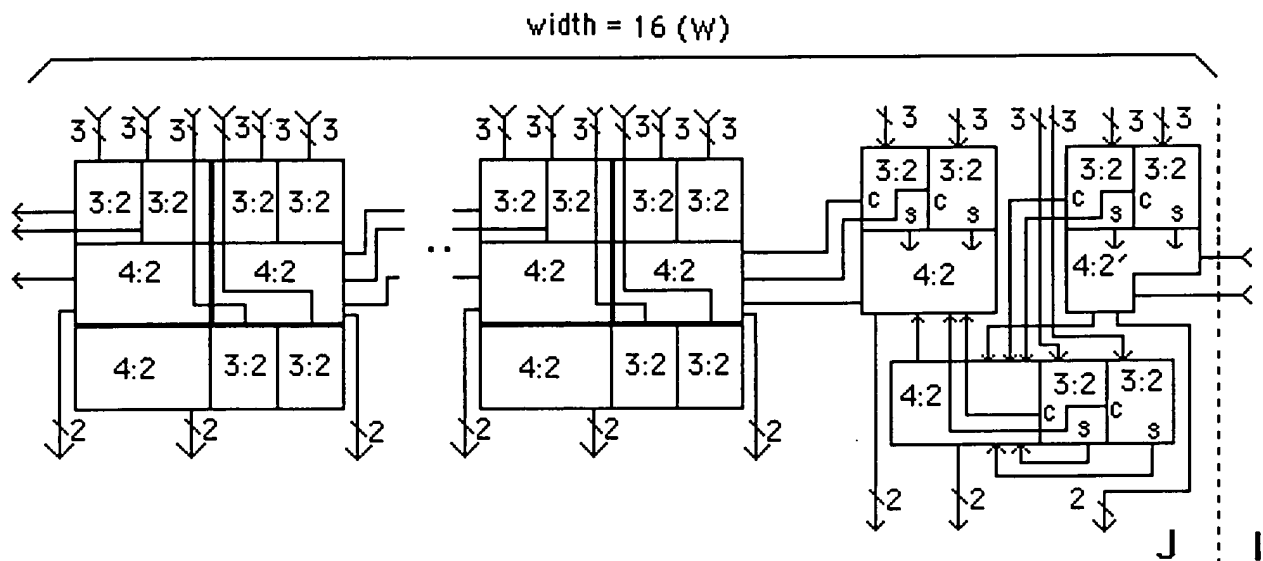


Figure 10B12. The layout draft for area J.  
(The same as area F except that it has two carry-in bits).



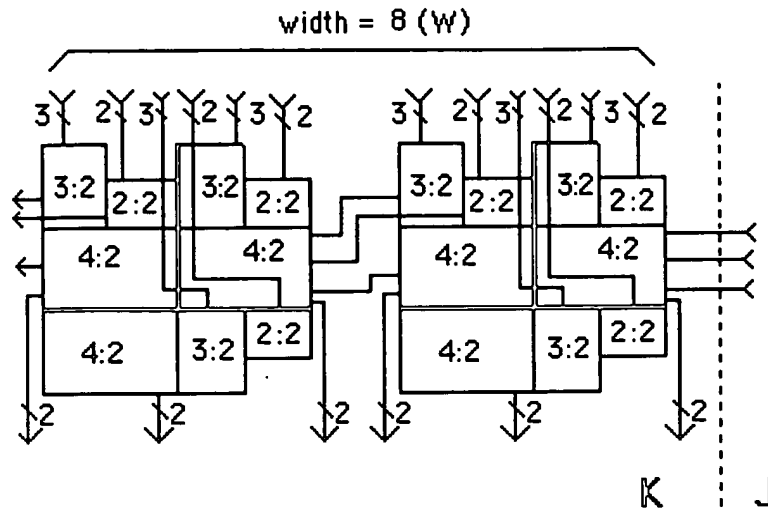


Figure 10B13. The layout draft for area K.

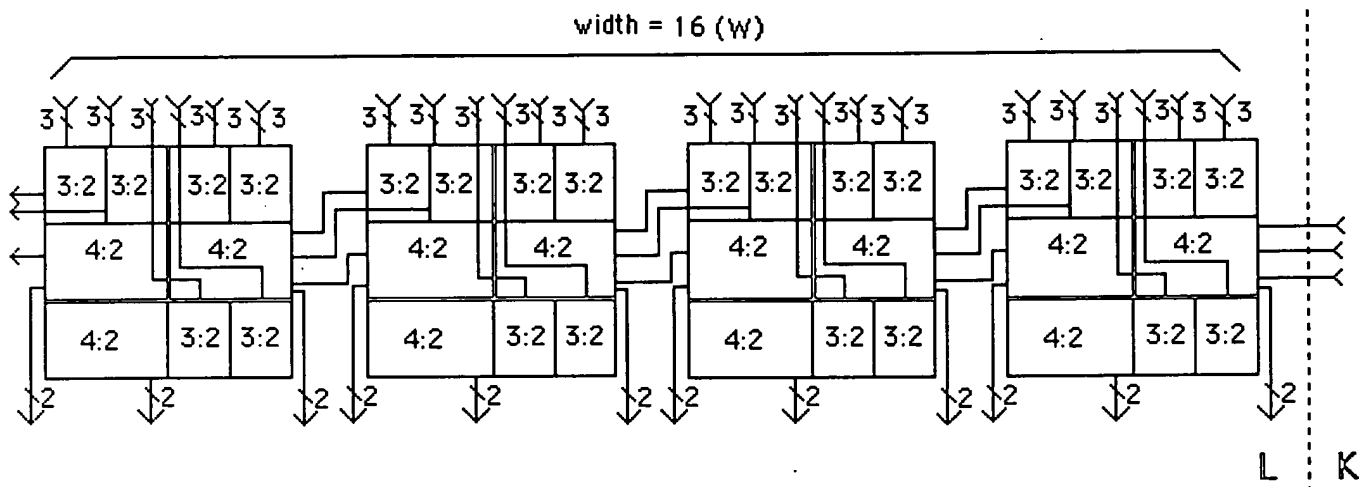


Figure 10B14. The layout draft for area L.

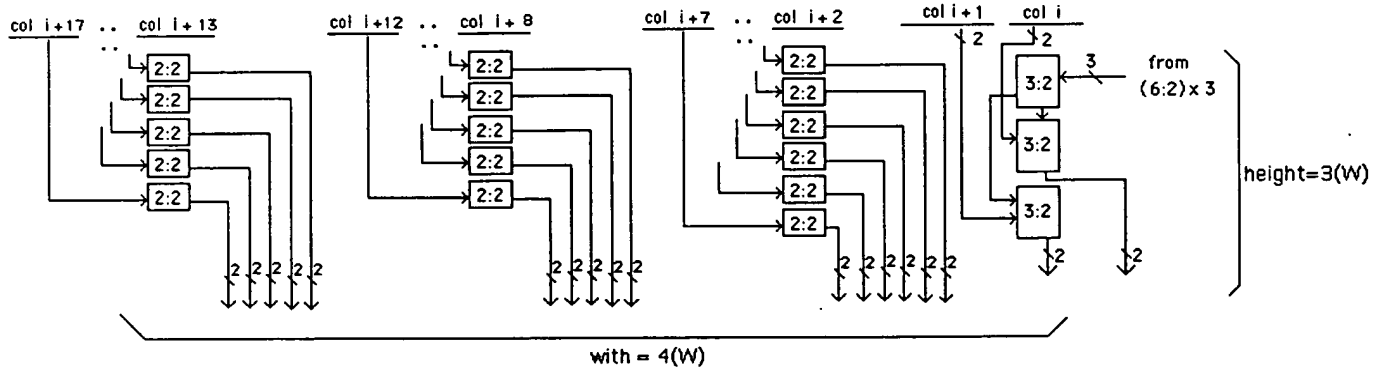


Figure 10B15. The layout draft for area M.



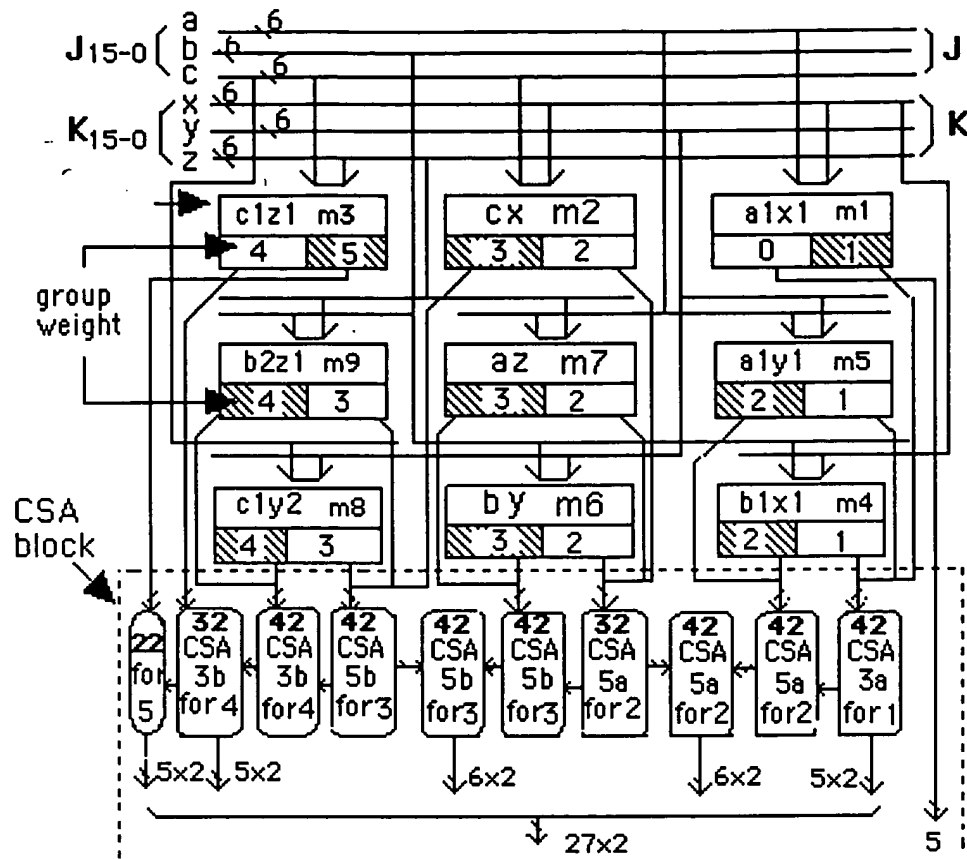


Figure 11C. The 16 x 16-b multiplier implementing  $(3m+1) \times (3m+1)$  for  $m=5$ .

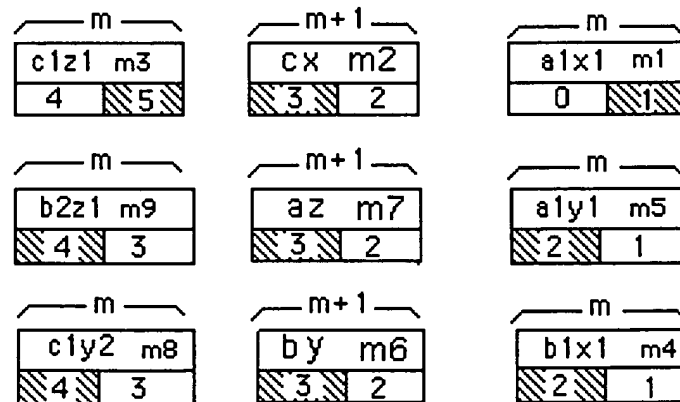


Figure 11D. The rectangular structure of the  $(3m+1) \times (3m+1)$ -b multiplier.

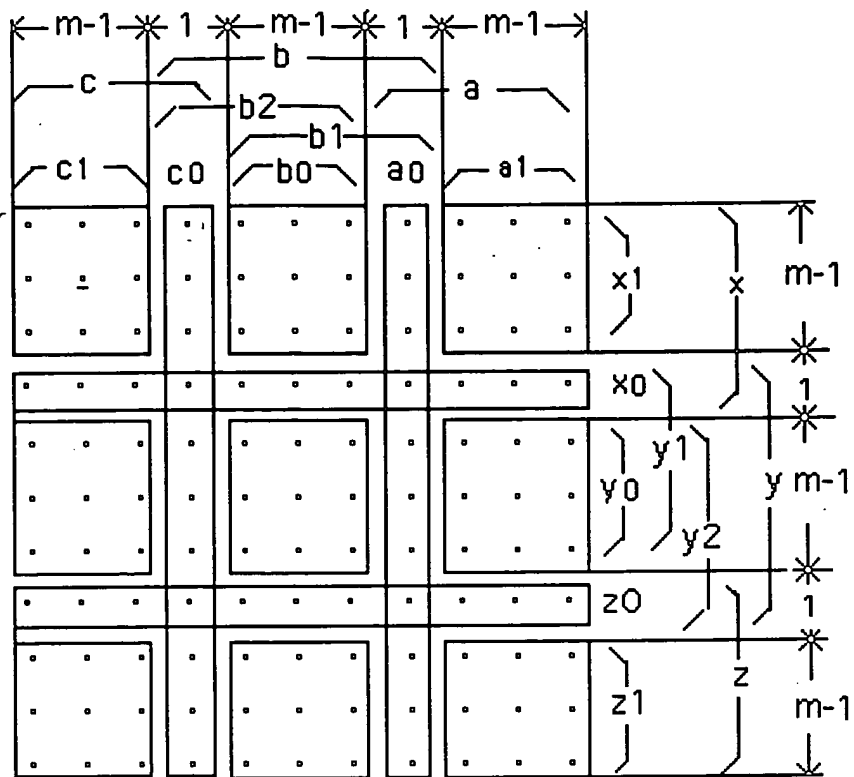


Figure 12A. The decomposition of  $(3m-1) \times (3m-1)-b$  ( $m=4$ ) bit matrix.

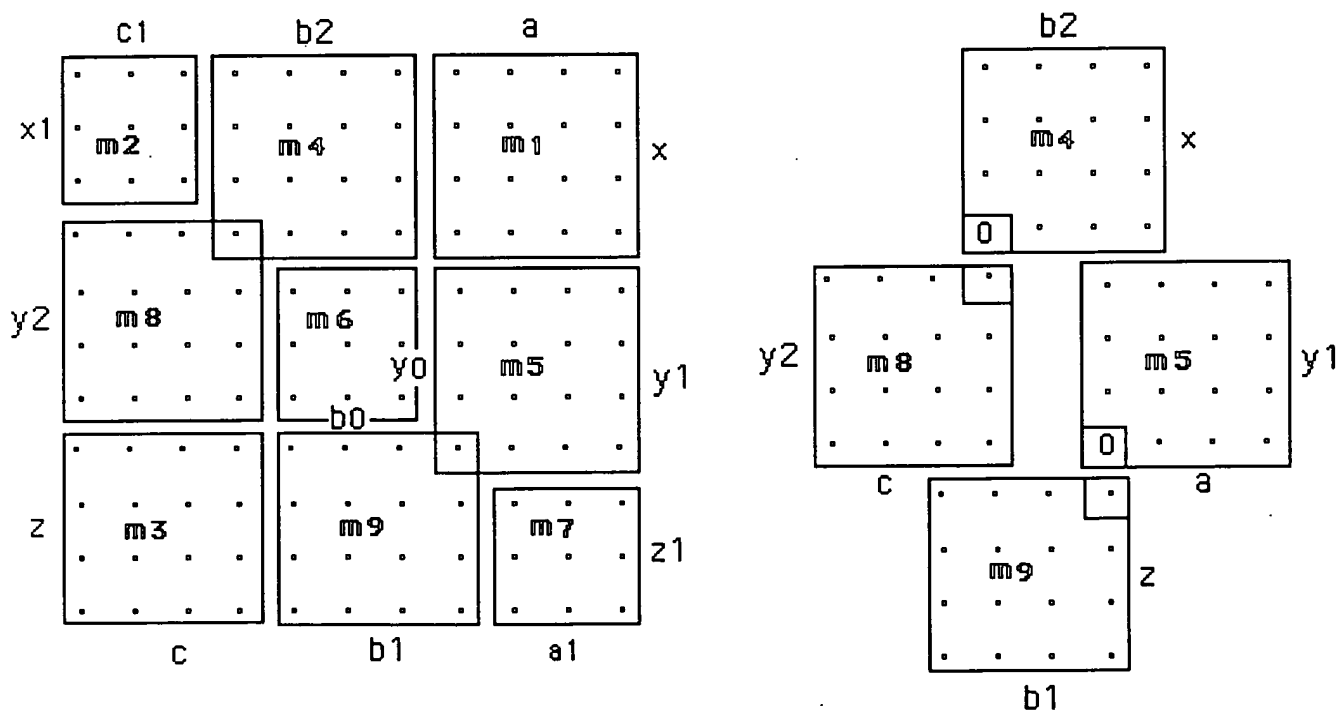


Figure 12B. The decomposition of  $(3m-1) \times (3m-1)-b$  ( $m=4$ ) partial product matrix.

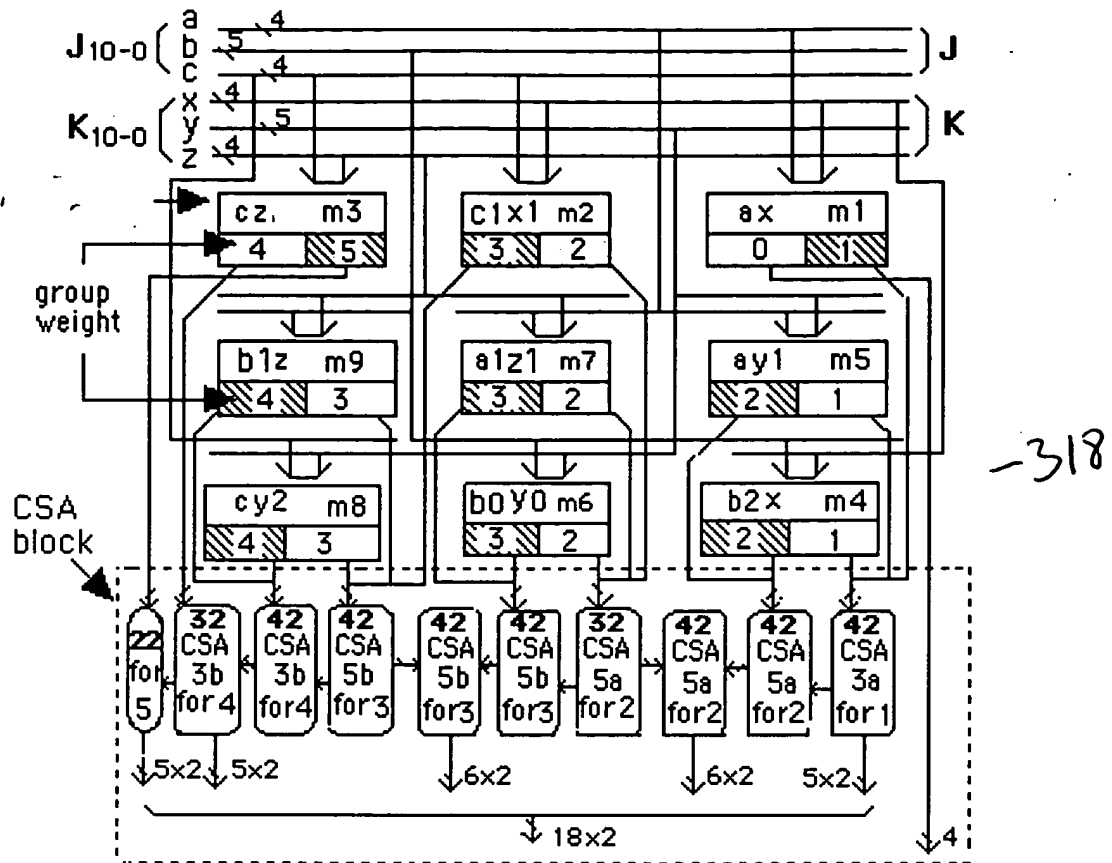


Figure 12C. The 16 x 16-b multiplier implementing  $(3m-1) \times (3m-1)$  for  $m=4$ .

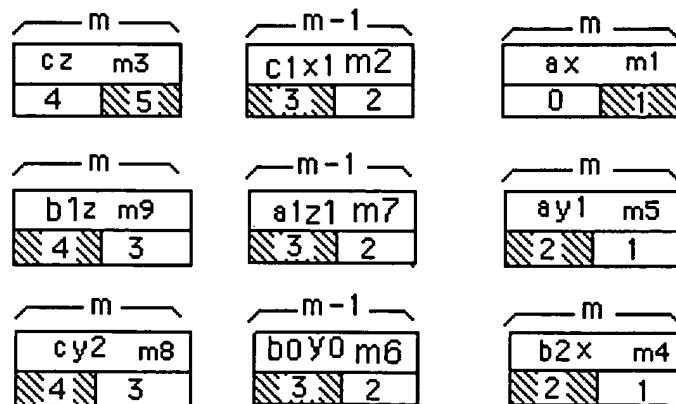
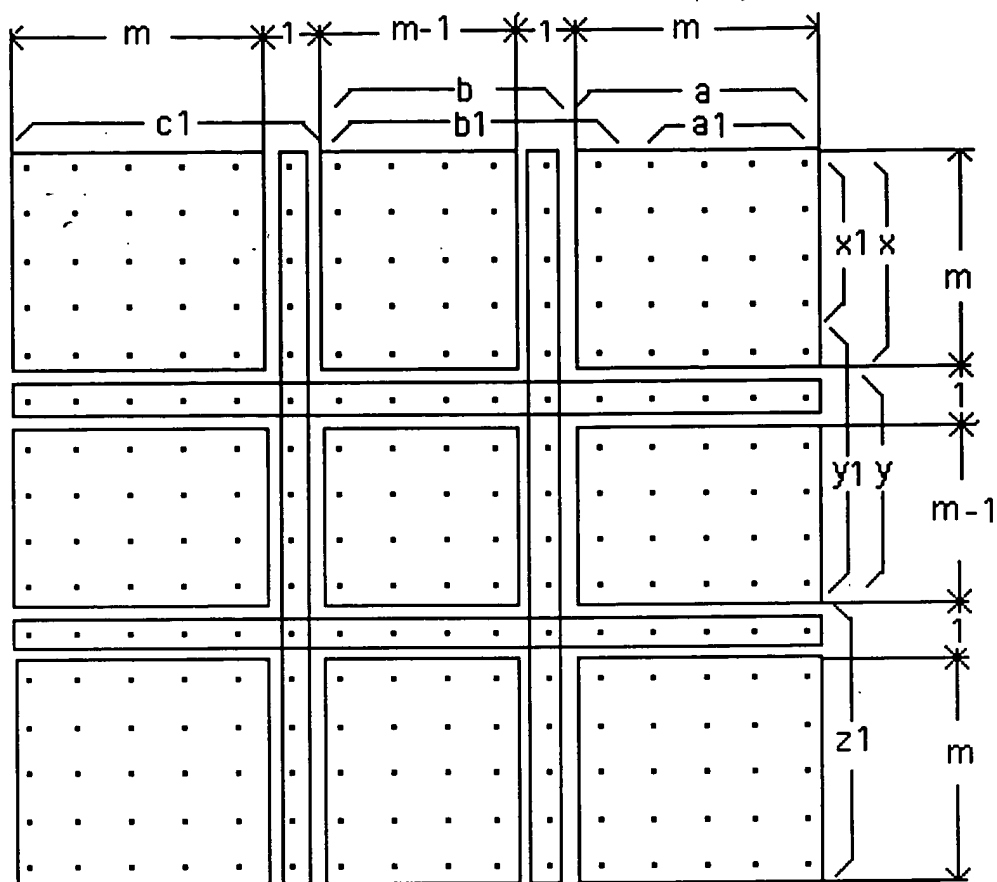


Figure 12D. The rectangular structure of the  $(3m+1) \times (3m+1)$ -b multiplier.



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Figure 13A. The modified decomposition of  $(3m+1) \times (3m+1)-b$  ( $m=5$ ) bit matrix.

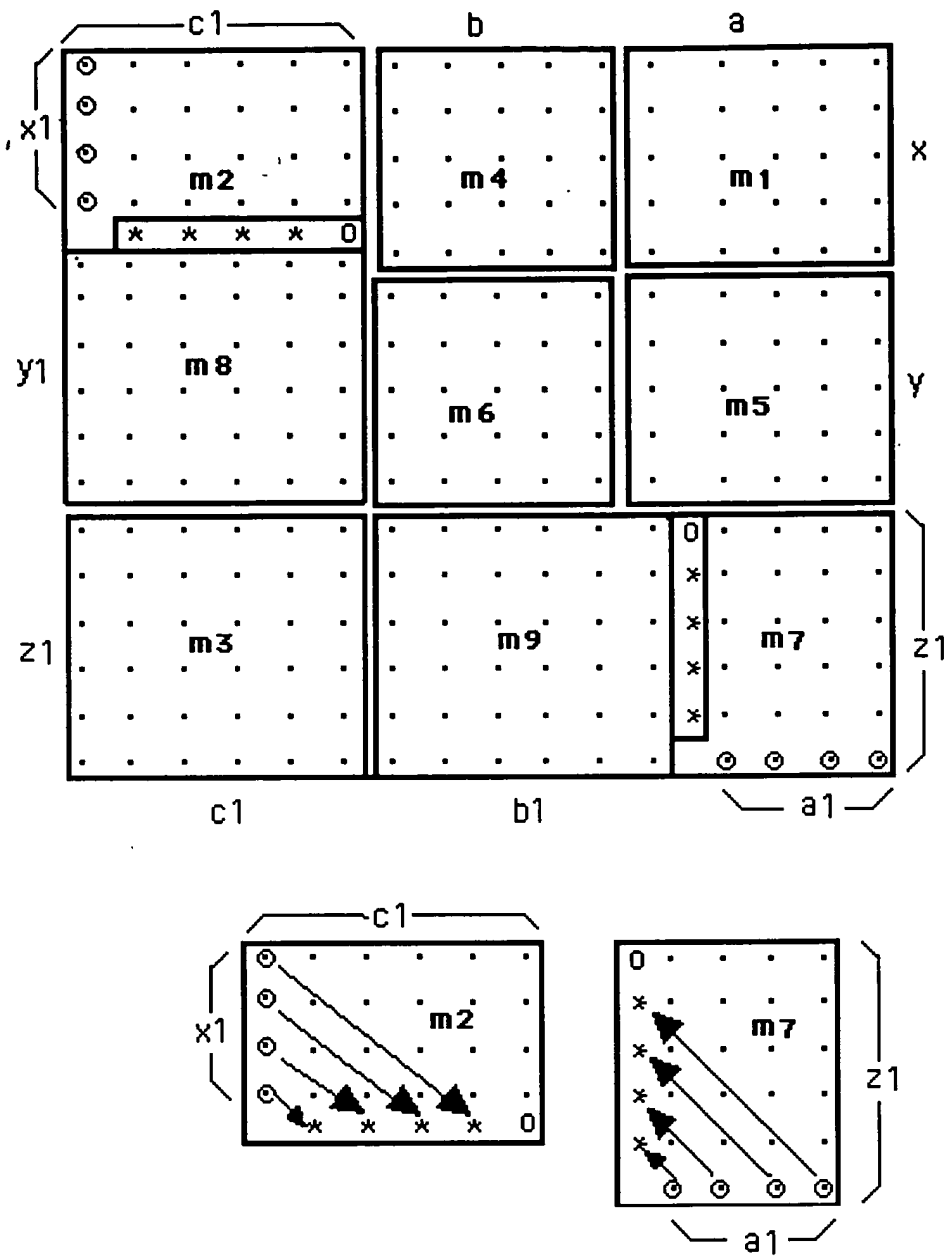


Figure 13B. The decomposition of  $(3m+1) \times (3m+1)-b$  ( $m=5$ ) partial product matrix modified from the decomposition of a  $3m \times 3m-b$  matrix.

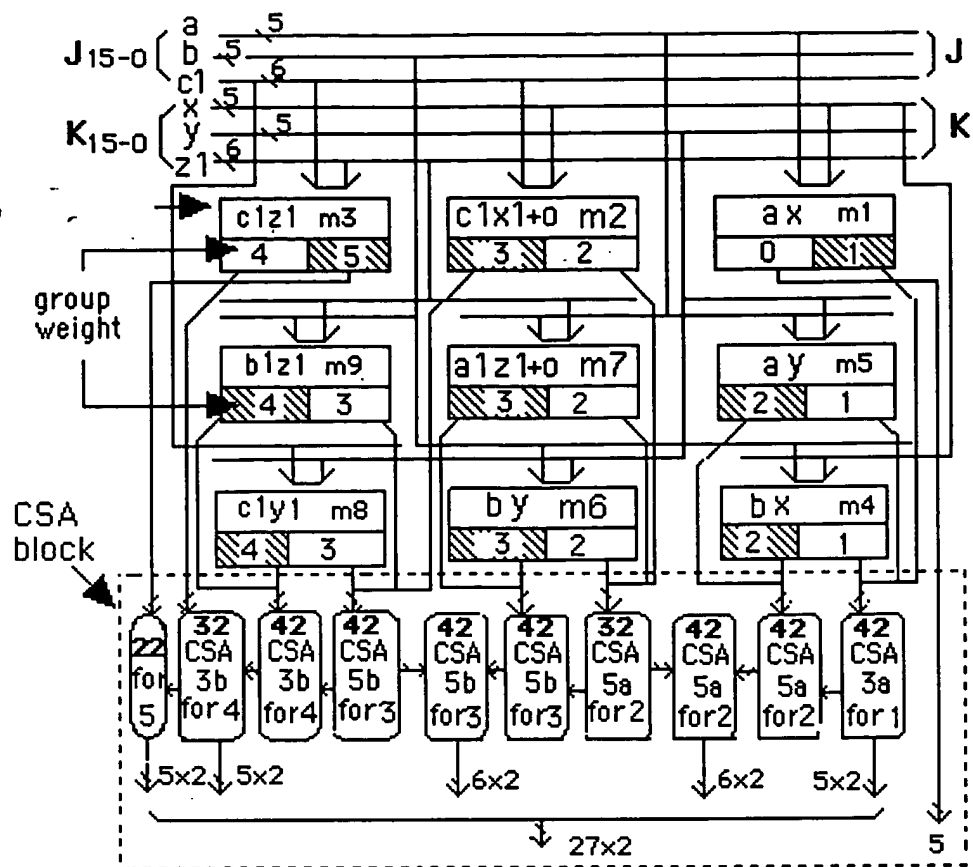


Figure 13C. The 16 x 16-b multiplier implementing  $(3m+1) \times (3m+1)$  for  $m=5$ , modified from the decomposition of a  $3m \times 3m$ -b matrix.





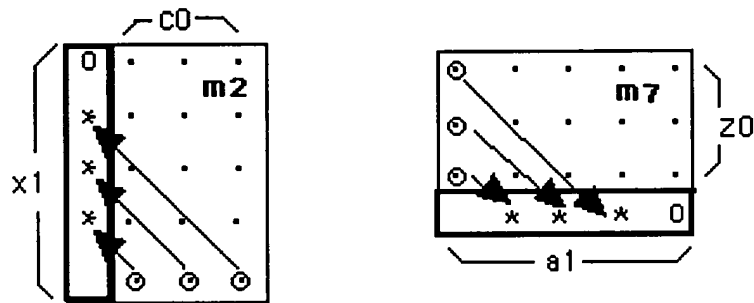
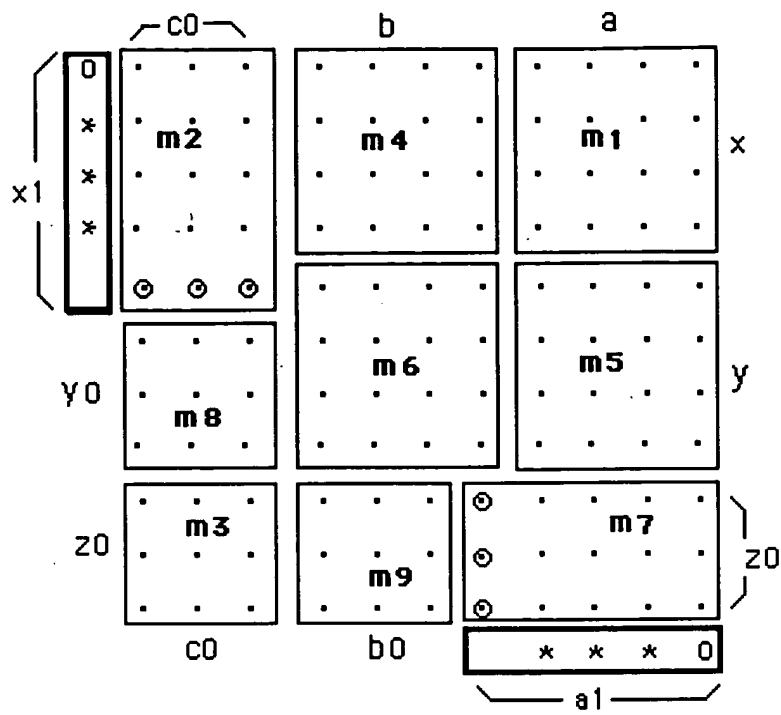
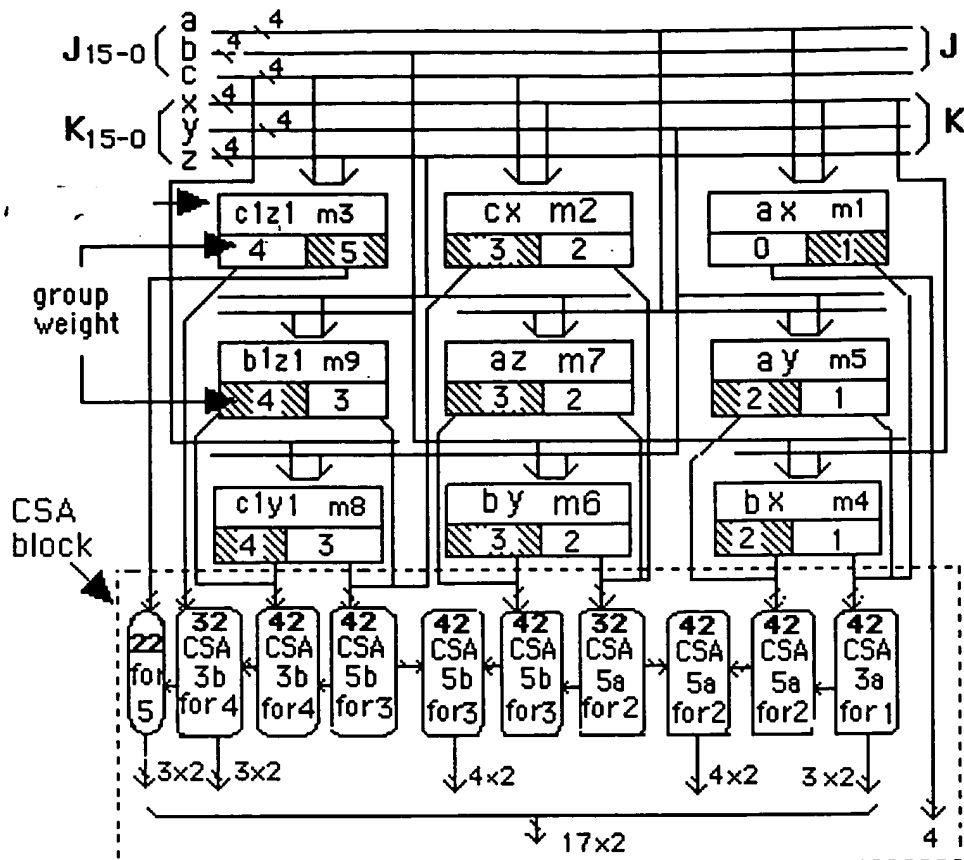


Figure 14B. The decomposition of  $(3m-1) \times (3m-1)-b$  ( $m=4$ ) partial product matrix modified from the decomposition of a  $3m \times 3m-b$  matrix.



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Figure 14C. The 11 x 11-b multiplier implementing  $(3m-1) \times (3m-1)$  for  $m=4$ , modified from the decomposition of a  $3m \times 3m$ -b matrix.

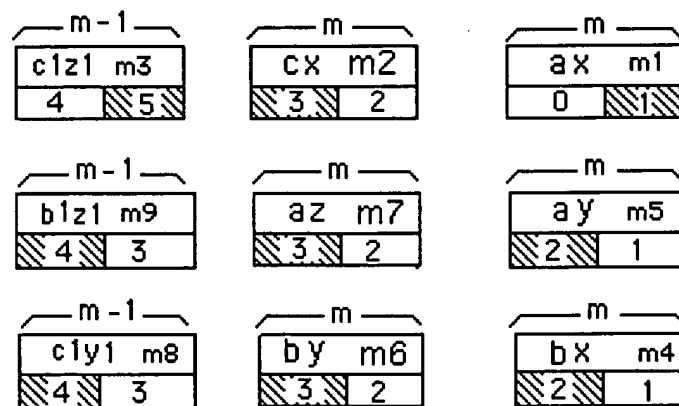


Figure 14D. The rectangular structure of the  $(3m-1) \times (3m-1)$ -b ( $m=4$ ) multiplier modified from the decomposition of a  $3m \times 3m$ -b matrix.